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Optical Communication Using Hybrid Micro Electro Mechanical Structures (MEMS) and Commercial Corner Cube Retroreflector (CCR)

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Optical Communication Using Hybrid Micro Electro Mechanical Structures (MEMS) and Commercial Corner Cube Retroreflector (CCR)

by

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DEDICATION

To my loving son, wife, parents and other family members who inspired me and stood by me to help me finish. I would like to dedicate my work to their sacrifice and support.

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The path to complete a doctoral research thesis is lengthy and grueling. During this journey of my dissertation, Dr. Scott Samson encouraged me, mentored me, and stood by me at each step. Without his advice and zeal for the technology, this research probably would not have happened. Scott has guided me, worked with me as a colleague, and provided candid opinion as a friend. This unwavering support means everything to me, and I don't think I can thank him enough for this.

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ABSTRACT

This dissertation presents a free-space, long-range, passive optical communication system that uses electrostatically modulated microelectromechanical systems (MEMS) structures coupled with a glass total internal reflection (TIR)-type corner cube retroreflector (CCR) as a non-emitting data transmitter. A CCR consists of three mirrors orthogonal to each other, so that the incident beam is reflected back to the incident beam, source. The operational concept is to have a MEMS modulator fusion with TIR CCR, such that the modulators are working periodically to disrupt the evanescent waves at the air interface of one of the three back glass faces of a TIR CCR. The MEMS chip has two primary components: (1) an array of movable light-scattering silicon structures with nano roughness and (2) a glass lid with a transparent conductive indium tin oxide (ITO) film. The MEMS structures are bonded to a glass lid using flip-chip bonding. Once bonded, the MEMS structures can be modulated either toward or away from the glass lid, thus disrupting evanescent energy delivered from a probing laser beam. The MEMS structure is precisely bonded to the TIR CCR with an accuracy of 10-30 arc-seconds using a Michelson interferometry feedback system. This is a novel step by which an existing passive commercial CCR can be converted into a modulating active CCR. This CCR-MEMS unit acts as the key element of the transmitter. To illustrate the concept of a low-power, unattended, sensor-monitoring system, we developed a sensor board containing temperature, humidity, and magnetic sensors along with a microprocessor and other electronics. The sensor board and CCR board are packed together and act as the transmitter unit. We developed a benchtop system and

an improved portable receiver system. The receiver system contains the laser (as source), a collimating lens (to collect retroreflected signal), an optical, narrow band pass filter, and a detector. The detector signal was amplified and filtered and sent either to the oscilloscope, a lock-in-amplifier, or a laptop to display the sensor data. Using the receiver system, a sensor-CCR-based transmitter unit, and receiver with 635 nm as source, we achieved retroreflective communication over a distance of 300 m.

CHAPTER 1

INTRODUCTION

Optical communication has been a mode of communication since medieval times. In the past, people used fire beacons to indicate an event, with eyes acting as receiver, and the beacon as transmitter [1]. Today, light sources such as light-emitting diodes (LED) or light amplification by simulated emission of radiation (laser) now have become the interrogating source and precise detector acts as receiver. If we need to convey only a trigger point or one specific event, optical devices like mirrors or reflectors can be used. For instance, the conveyer belt in a grocery store has a source/detector on one end and a reflector on the other, and the belt continues to run until an item interrupts the reflected signal. This system indicates an event (the item is there or not there), and the movement of the conveyer belt is based on the event. An automatic garage door uses a similar mechanism, with a reflector on one end and a source/detector on the other. If there is any obstruction between the source and reflector, the garage door does not close. Retro-reflectors are also used on streets so that drivers can clearly see the road.

1.1 Objective and Background

In the above examples, a reflector is used as a passive device to indicate a specific event. If we wish to perform optical communication using a reflector, we can design a mechanical shutter that blocks the light to indicate a binary position (say “0”) and pass the light to indicate the other position (“1”). Mechanical shutters controlled by digital electrical signals are easily available in the market and would be a one of the ways to perform optical communication. If the mirror has the right material, reflectivity, and performance, optical communication can be

performed over a long range for various wavelengths of interrogating sources. We can increase shutter speed to perform at high data rate communication. This system and setup are potentially useful at a macroscopic level, where the transmitter is larger than 3 cm^3, weighs more than 300 grams, consumes power in the mW-W region, and communicates in the 10- 100 msec range.

This macroscopic level setup may be good for some applications; however, applications such as inter-satellite communications, tags for inventory tracking, military applications, environmental monitoring, clandestine communication, and several others currently use active RF link communication. Using RF communication has drawbacks such as the possibility of jamming, bandwidth limitation, large antenna size, and high power consumption [2]. To overcome these drawbacks and have an alternative communication system, there presents a need for a compact (<1 cm^3), light (< 50 grams), low-power (µW – mW), high-speed (µsec – msec), cost-effective optical transmitter for long-range optical communication. This dissertation aims to provide insight in to one such compact, light, low power, high speed, cost effective optical communication method.

Micro electro mechanical systems (MEMS) is a renowned field in which mechanical or electrical actions are performed by providing actuation at the micron scale. Small devices in the range of 1 to 1000 µm are fabricated using the principles of semiconductor fabrication. The two major techniques used in MEMS fabrication are surface micromachining and bulk micromachining. In the former technique, layers of materials are deposited on a silicon wafer and etched to form MEMS devices. In the latter technique, the silicon wafer is etched and devices are formed. The field in which MEMS components are used for optical systems (MOEM) is an upcoming field, and several MOEM sensors are currently available in the commercial market. Texas Instruments' DLP mirror [3] and the deformable grating modulator developed at Silicon

Light Machines [4] are a few examples of optical MEMS systems. This dissertation describes the design of a MEMS chip that is precisely aligned to a commercial high-precision optical retroreflector, resulting in a transmitter that is used for optical communication.

1.1.1 Corner Cube Retroreflectors (CCR)

In the above examples the source and detector are on different sides. If we use one or two mirrors as the reflectors, then the positions of the source and detector are fixed, as for every incident angle there is a different reflected angle. This makes the sensor incident-specific, and the position of the detector becomes extremely crucial. In a CCR we use three mirrors that are orthogonal to each other and when the incident beam reflects off all three mirrors, then the retroreflected beam will be parallel to the incident beam, as shown in the optical ray from source to detector in Figure 1-1.

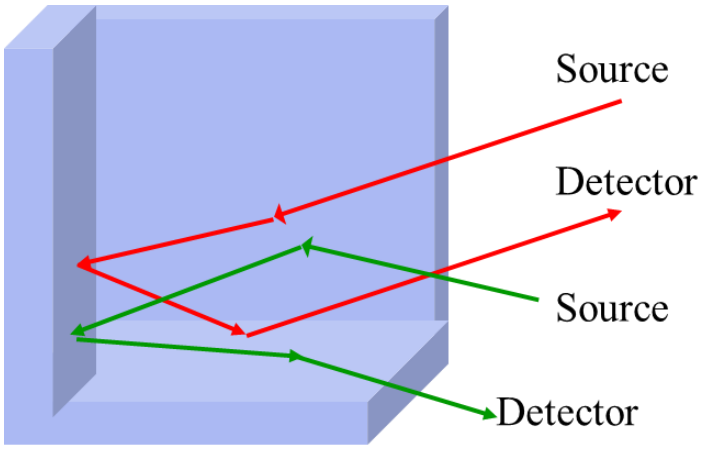

Figure 1-1: Hollow CCR

CCRs have found applications in numerous areas [2, 5-10]. For instance, an array of CCRs placed on the moon by Apollo astronauts [11] helps us determine the distance between the earth and moon at all times with great accuracy. One can measure the time it takes for the retroreflected beam to travel back from the base station at earth and depending on the light transmit time, one can estimate the distance between the base and the retroreflector on moon.

[11]. CCRs are readily available through commercial vendors like Thor Labs,[1] Edmund Optics,[2] and other optical vendors. CCRs are available in two major formats: hollow CCRs and total internal reflection (TIR) CCRs.

1.1.2 Hollow CCR

In hollow CCRs, three flat mirrors are precisely aligned and bonded perpendicular to one another as shown in Figure 1-1. Hollow CCRs with Au and Al coating are available for enhancement in specific wavelength ranges and come in various sizes. There is no bulk material absorption or chromatic aberration, as the optical path between the mirrors is in air [12, 13]. A hollow CCR has a wide range of acceptance angles, restricted only by the geometry of the entrance aperture, making it less affected to the angular position of the incident beam. Broadband hollow reflectors from Newport[3] have an acceptable incident beam range of 180° [12, 13]. Depending on the placement of the CCR, there is a chance it will be covered with dust and moisture if left outside, which may affect the intensity of the retroreflected beam.

1.1.3 Total Internal Reflection (TIR) CCR

In a TIR CCR, a solid piece of optical material (such as BK7) is polished, leaving a high-quality optical aperture and three orthogonal reflective faces (often these faces are coated with a metal to provide high reflectivity and acceptance angles similar to hollow CCRs) [12, 13] When uncoated, a CCR relies on the TIR effect to produce the three orthogonal reflectors. When the incident light angle exceeds the glass-air critical angle, then the incident beam is reflected within the CCR's glass, as shown in Figure 1-2. The limitation of the TIR CCR is that the range of acceptance angle is limited and dependent upon the refractive index of the glass.

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[1] Thorlabs Inc, Newton, NJ
[2] Edmund Optics, Barrington, NJ
[3] Newport, Irvine, CA

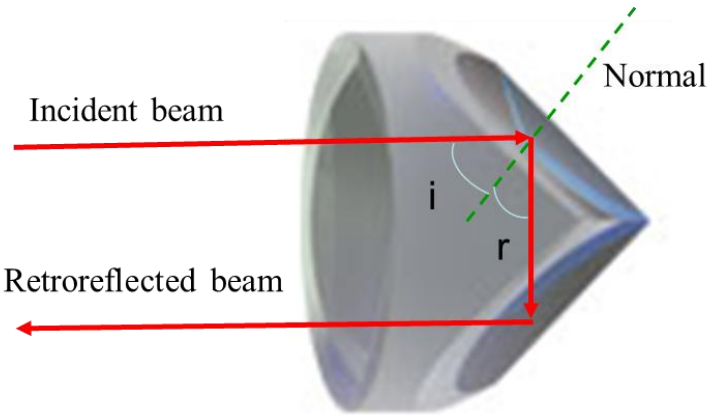

Figure 1-2: Total internal reflection CCR

1.2 Literature Review

The ability to retro reflect light back to the source makes CCR a lucrative optical device, one possibility is miniaturizing and bonding the mirror and having the ability to slightly misalign one of the mirror makes it a feasible research interest. Several research groups are looking to develop MEMS CCR for long range low power communication. One of the earliest research work to develop MEMS CCR used MEMS mirrors fabricated using a surface micromachined polysilicon MEMS process. Pister and his group designed hollow CCR in MEMS scale where two 250 μm square mirrors were designed and were vertically aligned using his special hinge technique [14], the third mirror had the ability to actuate using electrostatic actuation [6, 15]. The work demonstrated a communication range of 2 m using a 4.7 mW 670 nm laser at 500 Hz or 1k bps data rate and electrostatic voltage of 10-15 V to modulate the electrostatic mirror. Analysis was done to understand the key parameters required for long-range communication, non-flatness and misalignment of the mirrors seemed to be two major causes for low range of communication. The radius of curvature of the mirrors should ideally be ∞. For optical communication range of 1 km, it is required a radius of curvature of 50 cm or higher [6, 16, 17]. Misalignment of the mirrors seems to be their major limiting factor for long-range communication over1 km, the

mirrors need to be aligned by 0.5 mrad (103 arc-second) or better, and a receiver of 500 mm is required to collect the retroreflected signal.

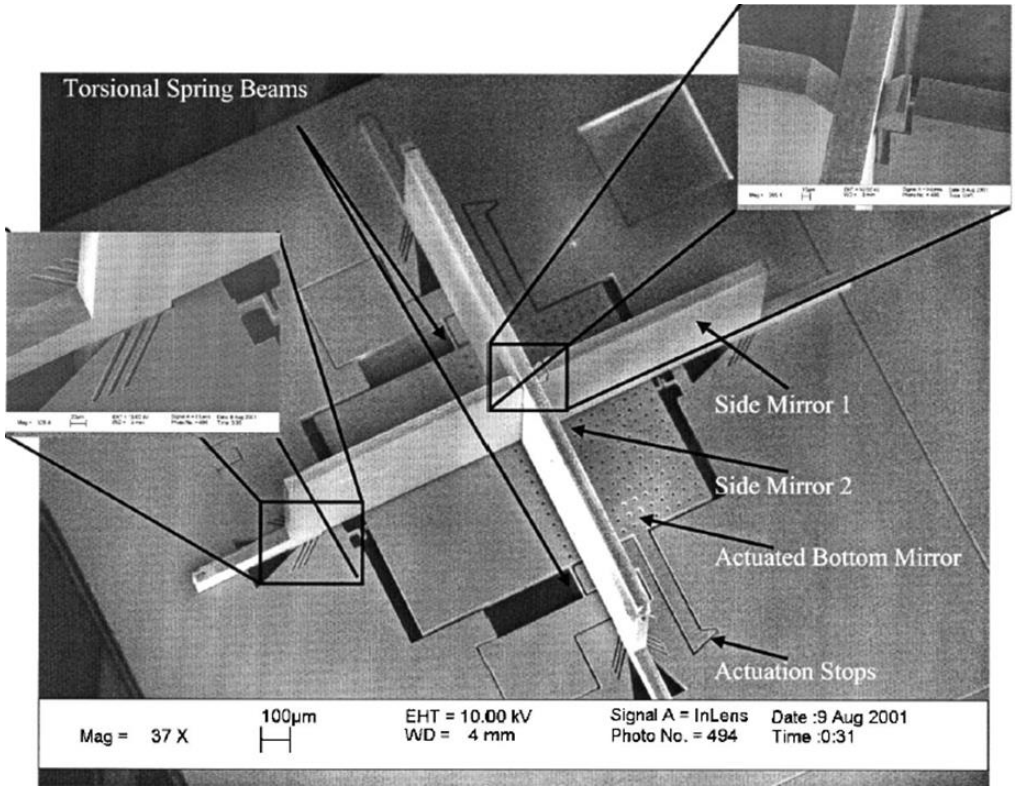

Figure 1-3[4]: Automated assembled MEMS CCR [17]

To improve mirror flatness, mirrors were later fabricated on single crystal silicon or structure layer of silicon on insulator (SOI) wafers. A thin layer of (50 nm) gold was deposited to improve the reflectivity of mirrors in some of the visible band. Initially the mirrors were aligned manually; later an automated alignment method was used. An alignment accuracy of less than 1 mrad (200 arc second) [6, 17, 18] was achieved on a 250-µm-square mirror. The electrostatic drive voltage was cut down from 10 V to 5 V and, using a 0.8 mW, 0.1 mrad (20 arc second) divergence, 632.8 nm laser, communication of 180 m was achieved at 200 Hz or 400 bps [17,

[4] Image was published in IEEE Micro Electro Mechanical System 2002, DOI: (10.1109/MEMSYS.2002.984332) and permission to use is included in Appendix A

18]. An order of magnitude improvement in communication range was made from the previous version to the current version. Energy consumption of 19-40 pJ per bit was reported, and total power consumption of the system was 1.7 mW [17]. This concept of developing a MEMS based CCR on electrostatic actuation method for unattended sensor monitoring concept from the above group was bought by a commercial company that intended to do low-power node-to-node communication using the MEMS CCR, to provide power to the CCR chip along with sensors it was bonded to a CMOS IC and solar cell array in a 16 mm^3 form factor [18].

In another publication, a self-assembled method using melting of resist was used to assemble the mirrors of the CCR. The CCR mirrors were aligned with an accuracy of 0.18° (~ 650 arc second) [19]. The drive voltage for these self-assembled mirrors fabricated using bonded silicon on insulator (BSOI) wafers had an actuation voltage of 30V and signal to noise ratio of 30 dB [19]. The communication range performance of the fabricated CCR was similar to that of the previously mentioned CCRs.

Similar to the above style of CCR, one of the groups fabricated piezoelectric actuators as the horizontal mirrors. They fabricated 300-µm vertical mirrors by etching doubly bonded SOI wafers using KOH. These vertical mirrors were then diced and manually bonded to horizontal mirrors. A novel design minimized the effect of residual stress from the PZT film on the horizontal mirrors, and a 5 V signal on the horizontal mirror was sufficient to displace the mirror by 1.37°. Alignment accuracy of 0.13° (~450 arc second) between the mirrors was reported, and an optical communication of 5 m at 2.5 kHz was achieved [20].

One of the groups working on long-range communication used a TIR CCR and developed a technique using multiple quantum well modulators (MQWM). Modulators were fabricated using layers of InGaAs/InAlAs quantum well on InP. The transparency or color of the

film (well) changed when voltage (15 V) was applied. This MQWM was attached to a 0.63-cm-diameter commercial TIR CCR with 10 arc second (0.048 mrad) alignment accuracy. A communication range of 2 km at 5 Mbits/s (~ 2.5 MHz) was achieved using a 1550 nm laser operating at 4.2 W. A set of five modulators was arranged in a mechanical fixture, and 2 km communication was demonstrated across Chesapeake Bay, with each modulator consuming 200 mW [7, 21, 22]. Although this method has a long range of communication, using an electro-optic modulator consumes a lot of power (0.2 W per modulator compared to 1.7 mW electrostatic actuation of a MEMS mirror).

One of the other groups used an array of TIR-based CCRs and applied pressure on an elastomeric material, such that the elastomeric material is close to one of the reflecting mirrors of the TIR CCR. A thin film close to the mirror causes frustration of the total internal reflection, which reduces the intensity of the retroreflected signal. A 0.9 m CCR array was selected and 2% carbon loaded PDMS gel was used as the elastomeric material. Pressure of 100 kPa was applied to the film, and a 1% change in retroreflectance was observed [23, 24]. This process was slow and inconsistent because the gel took time to bond and debond to the CCR when pressure was applied.

One of the research groups demonstrated the use of CCR in a magnetometer application, where a change in magnetic field between 820 A/m and 6 kA/m was detectable. A hollow MEMS CCR was fabricated with one of the mirrors on a movable torsion arm connected to a magnet. As the magnetic field changed the torsion arm would move, causing the movable CCR mirror to deflect from its original position. This application is suitable for detecting large amounts of ferrous material (e.g., jeeps, tanks, weapons) [8].

Several research groups have been working on understanding the challenges in long-range optical communications, such as atmospheric turbulence and incident beam divergence. One researcher illustrated that in a retroreflected beam based communication system the retroreflected beam spot has a standard deviation of about 1 cm for a communication of 300 m and about 10 cm for a communication up to 500 m in turbulent measurement conditions [25-27] and suggested that the effect of turbulence on the beam spot becomes significant as the range exceeds 1 km. Other groups have focused on different communication schemes, and one researcher suggested that using an on-off keying method and array of reflectors with one photodiode to receive all the retroreflected signal would yield better signal-to-noise ratio (S/N) than multiple detectors[28-31]. One of earliest papers describing communication through retroreflected power concluded that the S/N of optical communication would be better than that of radar communication [2, 29, 30].

1.3 Previous Work at USF

In our earlier work at the University of South Florida, we started with a hollow MEMS CCR, where the vertical mirrors were fabricated using deep reactive ion etching (DRIE) etching of a double side polished silicon substrate. To improve the flatness and roughness of the DRIE surface, they were treated with KOH+IPA etching. Finally they were metallized and bonded to a single side polished silicon wafer with horizontal mirror. Using bulk micromachining we fabricated electrostatically actuated mirrors using a custom developed process called NitrideMEMS. In this process, 2-μm silicon nitride was the structural material with a sacrificial gap of 3 μm. Top and bottom electrodes were deposited using Cr/Au or Ti/Au layers. A completely fabricated MEMS CCR is shown in Figure 1-4. Using this process, we fabricated the CCRs with alignment accuracy of 0.1° and surface roughness of 10 nm [32]. We achieved a

communication range of 10-30 m at 1 kHz data rate and applied actuation voltage of 6 V on the mirrors to move the mirrors from on to off position [5, 32-35].

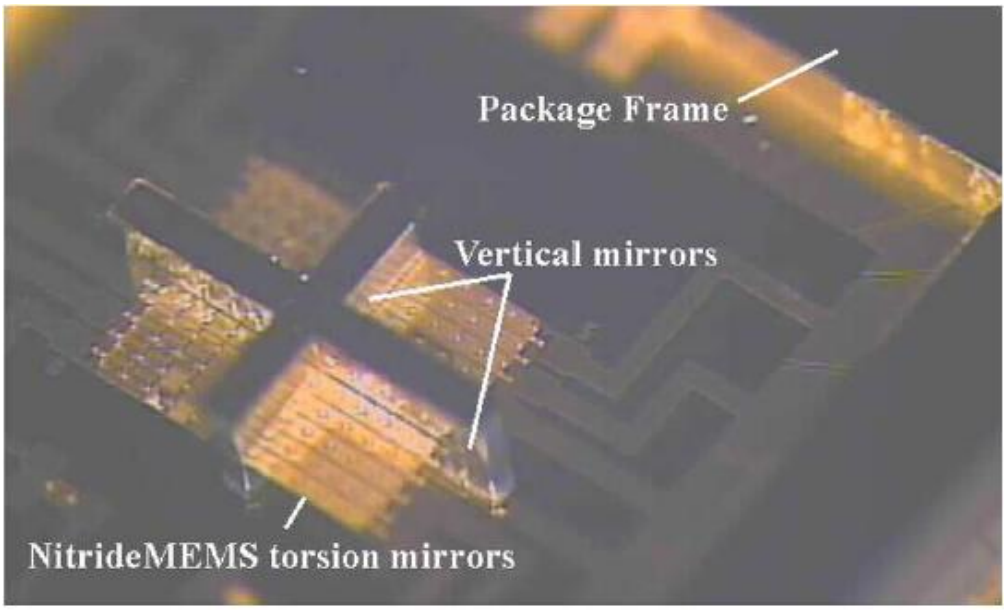

Figure 1-4[5]: Hollow CCR fabricated with 250-µm-long vertical mirror and movable horizontal mirror [32, 33]

A transmitter unit 30 x 30 x 6 mm was designed to incorporate the CCR, mechanical switch, microprocessor, temperature/humidity sensor, indicator LEDs, and thin batteries as shown in Figure 1-5. The unit met all the above-mentioned criteria except the communication range; this was because the misalignment of mirrors in this system was ~0.5°, which was sufficient to cause the retroreflected signal to be undetected after 30 m [5, 32, 36].

From the research mentioned above and the literature review, we realize that miniaturizing traditional hollow CCRs using MEMS concept was difficult. As aligning the MEMS mirrors to precise orthogonality was a major issue, causing low communication range. When TIR CCRs were used with a MQWM modulator, they were able to communicate over long

[5] This image was published in IEEE MEMS, NANO and Smart Sensors 2005, DOI: (10.1109/ICMENS.2005.50) and permission to use is included in Appendix A

ranges but consume many watts of power. The work presented in this dissertation illustrates a different approach taken to improve the communication range and develop a compact (1 cm^3), low-power (10 mW), moderate data rate (5 kHz) optical communication system.

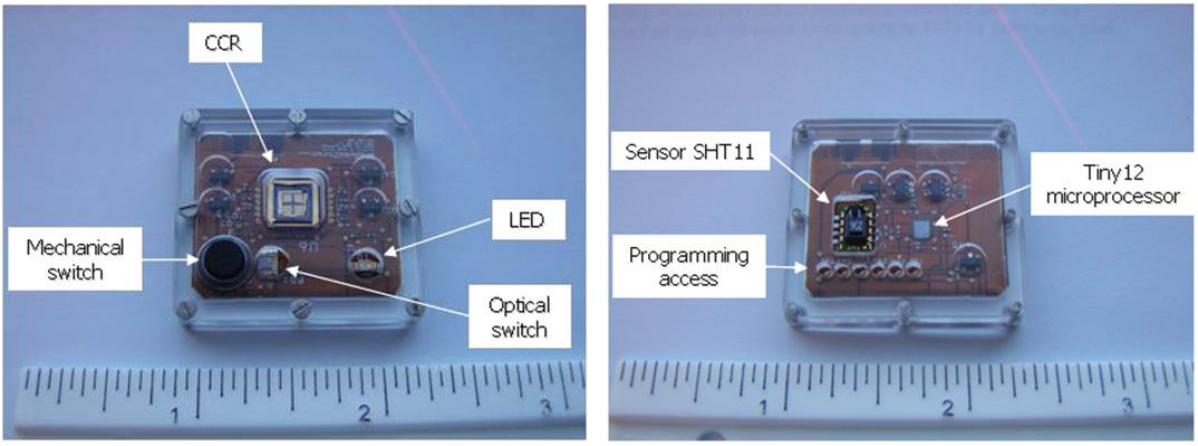

Figure 1-5[6]: Front and back side of a packaged MEMS CCR with temperature sensor [36]

1.4 Organization of the Dissertation

This dissertation is divided into four major parts: transmitter and receiver design calculations, design and fabrication of MEMS chip for transmitter; bonding and testing and development of hybrid MEMS-CCR transmitter; and development of the receiver unit and improvements. In the second chapter we discuss the CCR selected and the concept of evanescent wave coupling, empirical calculations for design of transmitter and receiver system. Chapter 3 details the process development, followed by design and fabrication of the MEMS chip. Chapter 4 discusses in detail testing of the fabricated MEMS structure and then the precise bonding of the MEMS and CCR and benchtop optical testing results. Chapter 5 discusses the development of transmitter/receiver unit and improvement made in the MEMS chip and optical communication results. Finally, chapter 6 concludes the discussion and provides future recommendations.

[6] This image was published in SPIE Defense and Security, 2007. DOI: (10.1117/12.721203) and permission to use is included in Appendix A

CHAPTER 2

DESIGN AND CALCULATIONS OF OPTICAL, MEMS CHIP AND SYSTEM PARAMETERS

In the previous chapter, we learned that several researchers are looking to develop a compact, low-power, high-speed, lightweight transmitter for optical communication. The CCR has been identified as one of the key transmitter components, and most research uses a traditional MEMS method to fabricate and assemble the reflectors. We also plan to use MEMS technology to assist us in creating a transmitter with those important qualities to perform long-range optical communication. However, our approach uses a MEMS chip hybridized with a commercial CCR. In this chapter we first lay out the key CCR parameters for long-range communication and then explain our MEMS technology and commercial CCR hybrid concept for the transmitter. Next, we discuss the CCR selection. Finally, we perform optical and electrical calculations to design the optical system and the MEMS chip.

2.1 Factors Impacting Range in a CCR-Based Communication System

Numerous factors play an important role in determining the range of an optical communication system based on CCR. Source wavelength, acceptance angle, mirror roughness, mirror coating, and atmospheric turbulence all affect communication range, but the two most important factors that dictate the range of optical communication are orthogonality and flatness of the mirrors, as discussed below.

2.1.1 Orthogonality of the Mirrors

A CCR has three mirrors, and the relative orthogonality of these mirrors is extremely critical for long-range optical communication. Commercially available CCRs have orthogonality (or misalignment) accuracy between the three mirrors of 1-10 arc-seconds (0.00277°), almost 20 times better than any reported MEMS CCR device. It is extremely challenging to fabricate a miniature MEMS-based CCR with one active (movable) mirror and align them to an accuracy of 1-10 arc second (0.00277°). This level of alignment accuracy is important because it enables capture of the retroreflected signal with a reasonable size detector [16, 37]. As illustrated in Figure 2-1, if the CCR has a misalignment (δ), then for an optical communication range of *L*, the offset (*x*) of the CCR's retroreflected signal due to misalignment is represented as

$$x = L\,tan\delta. \tag{2.1}$$

If we are able to bond the CCR mirrors with an accuracy of 30 arc-seconds, then for an optical communication distance of 1 km, the offset in the retroreflected signal would be 145 mm, which means that at least a 145 mm wider detector is required to capture the retroreflected signal (this is without considering beam divergence). As seen in Equation 2.1, the misalignment in the mirrors directs the detector size. A 10-30 arc-second misalignment enables a reasonably sized (145 mm) receiver optics that can capture most of the retroreflected signal.

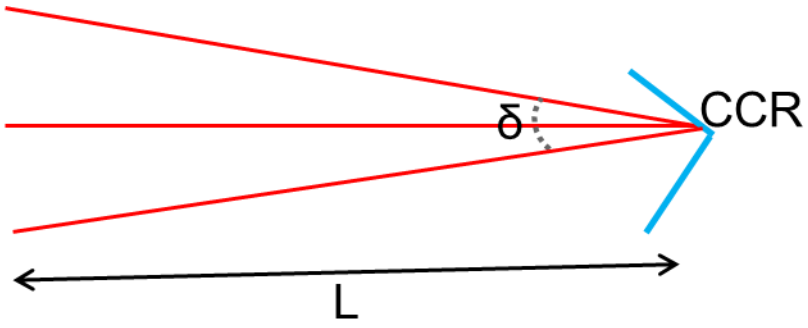

Figure 2-1: CCR mirror misalignment causing the retroreflected signal to disperse at long ranges

2.1.2 Flatness of the Mirrors

The second most important factor in determining optical communication range is the flatness of the mirrors. The researchers at UC Berkley [6, 16, 17] performed optical modeling and determined that CCR mirrors need to have a 100-cm radius of curvature for optical communication over 1 km. Their paper explains that if the radius of curvature of the mirror is below 50 cm, then the quality of the retroreflected signal diminishes significantly, and that below 20 cm, the mirror is not suitable for long range optical communication. The paper compares retroreflected signals from four different radii of curvature: 20 cm, 50 cm, 100 cm, and ∞ and concludes that a 50-cm curvature gives a 1.5x improvement in the amplitude of the retroreflected signal, and that using a mirror with a 100-cm curvature creates a 2x improvement as compared to a mirror with a 20-cm radius curvature. A mirror with infinite curvature is an ideal mirror, and it retroreflects the beam entirely. Commercial CCRs are available with curvatures from 100 cm to ∞; in our design we plan to use mirrors with a radius of curvature better than 100 cm.

2.1.3 Other Factors

Source wavelength, CCR material, incident angle, size of CCR, incident laser power play an important role in determining the system parameters. However, these are external factors and can be altered to make the overall communication system effective. We will discuss more about these factors and their impact in later sections. Weather conditions and suspended air particles in the atmosphere causes attenuation and scattering of the retroreflected signals. The Mie scattering model [7, 25, 26, 38], examines how environmental conditions affect line-of-sight optical communication, at different ranges. One of the researchers developed a model to illustrate how turbulence affected the retroreflected signal, and concluded that there is deviation of beam by 1 cm at 300 m and 10 cm at 500 m [25, 38].

2.2 CCR MEMS Hybrid Concept

From factors discussed above, we have concluded that there is a tight tolerance on the misalignment of the mirror and that the idea of making a completely MEMS-based CCR system with one movable mirror while maintaining precise orthogonality during the off state would be extremely challenging. Micromachining techniques provide an advantage by allowing the fabrication of miniature electro-mechanical structures. Commercial CCRs offer the precise alignment essential for long-range communication. By combining these two advantages, we can develop a hybrid commercial CCR-MEMS unit that will decrease the retroreflected signal in one state and allow it in another. Figure 2-2 illustrates such a unit.

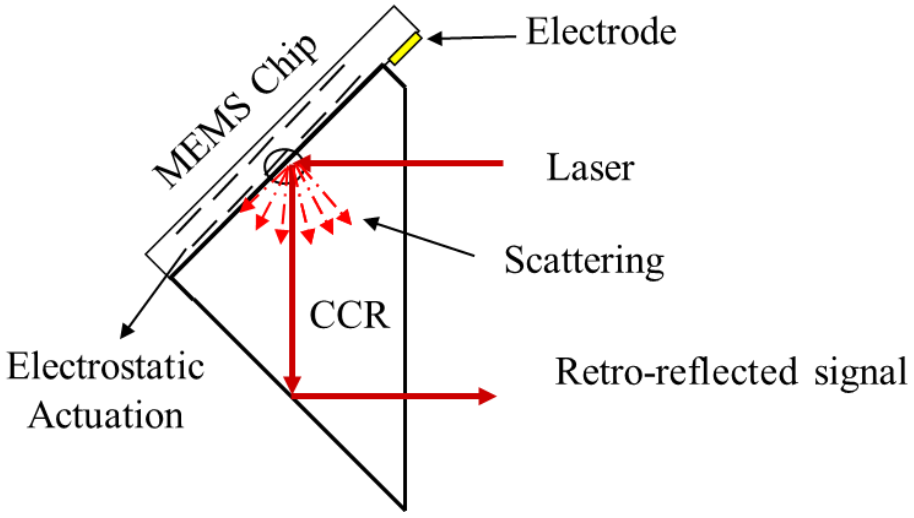

Figure 2-2: Commercial CCR and MEMS chip concept

The idea is to develop a MEMS chip that can precisely bond to the TIR-based CCR and shift (or extend) the retroreflecting plane of the TIR so that a MEMS structure can, upon actuation, be brought close enough to attenuate the retroreflected signal by scattering the light at the extended surface. Electrostatic actuation is one of the methods we can use to position the MEMS structures close to the new TIR plane; we can also devise MEMS structures that will interact with the surface waves. We plan to pursue this concept by increasing our understanding

of the optical requirements for the communication system and then determining the requirements to develop the MEMS actuator.

2.2.1 Principle of TIR and Evanescent Wave Coupling

Total internal reflection (TIR) occurs when an incident light from above the critical angle passes through a medium of higher refractive index into a medium of lower refractive index, causing all the light to be reflected at the boundary of indices. During reflection at the glass-air interface, evanescent waves are formed in the air near the surface of the glass (Figure 2-3). These evanescent waves decay exponentially perpendicular to the reflection plane, as represented in Equation 2.1 [39-41]. If not disturbed, the evanescent waves then reflect back along with the internal reflected beam. If we disrupt these evanescent waves, then the intensity of the retroreflected beam diminishes. This attenuation in the reflected signal illustrates the difference between the un-scattered and scattered mode. Since bonding the MEMS structure close to the TIR plane is not possible, a glass lid with MEMS structures capable of moving in-and-out of plane was bonded to one of the sides of TIR CCR. The glass lid can also provide inherent environmental protection to the modulating MEMS structures.

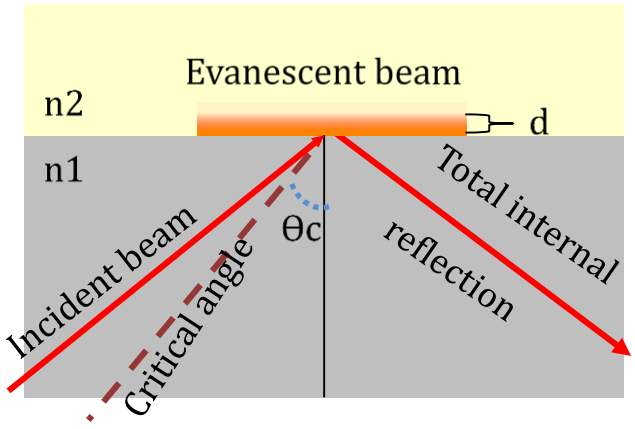

Figure 2-3: Total internal reflection occurs when the incident angle is greater than the critical angle.

$$I(z) = I_o e^{-z/d} \tag{2.2}$$

$$d = \frac{\lambda_i}{4\pi n_1 \sqrt{\sin^2 \Theta_i - \sin^2 \Theta_c}} \tag{2.3}$$

$$\Theta_c = \sin^{-1}\left(\frac{n2}{n1}\right) \tag{2.4}$$

We understand that the evanescent waves occur close to the surface and decay exponentially as from Equation 2.2 [37, 39, 40, 42]. To calculate the depth of penetration for waves in perpendicular distance *z* from the interface, let us consider Equation 2.3 [37, 39, 40], where *d* is the penetration depth of the waves, λ_i is the wavelength of the incident beam, Θ_i is the incident angle, Θ_c is the critical angle, *n1* is the refractive index of BK7 is 1.515 for 635 nm light, and *n2* is the refractive index of air (1 for all wavelengths). The critical angle can be calculated from Snell's law using Equation 2.4 [40]. Using the data mentioned above calculations show a critical angle of 41.3° for a wavelength of 635 nm. Penetration depth of the evanescent waves for a 635 nm source, for instance with an incident angle of 43° is 195 nm, and this evanescent wave decay increases as the incident angle becomes closer to the critical angle. By bringing the MEMS scattering structures within the penetration depth, we can disrupt the evanescent beam and reduce the intensity of the retroreflected beam. This scattering of evanescent waves forms the basis of our modulator's operation.

2.2.2 Determination of Penetration Depth for Different Wavelengths

To understand how fast the evanescent beam decays and what effect it has on the retroreflected signal we can compute that from Equations 2.2 and 2.3, one of our colleagues developed a MATLAB program using a more detailed analysis mentioned in Book: *Principle of Optics* [40]. This program is to compute reflection of an incident beam (at 45°) on a mirror when a scattering object is bough in the close vicinity (defined as gap) to the reflection plane.

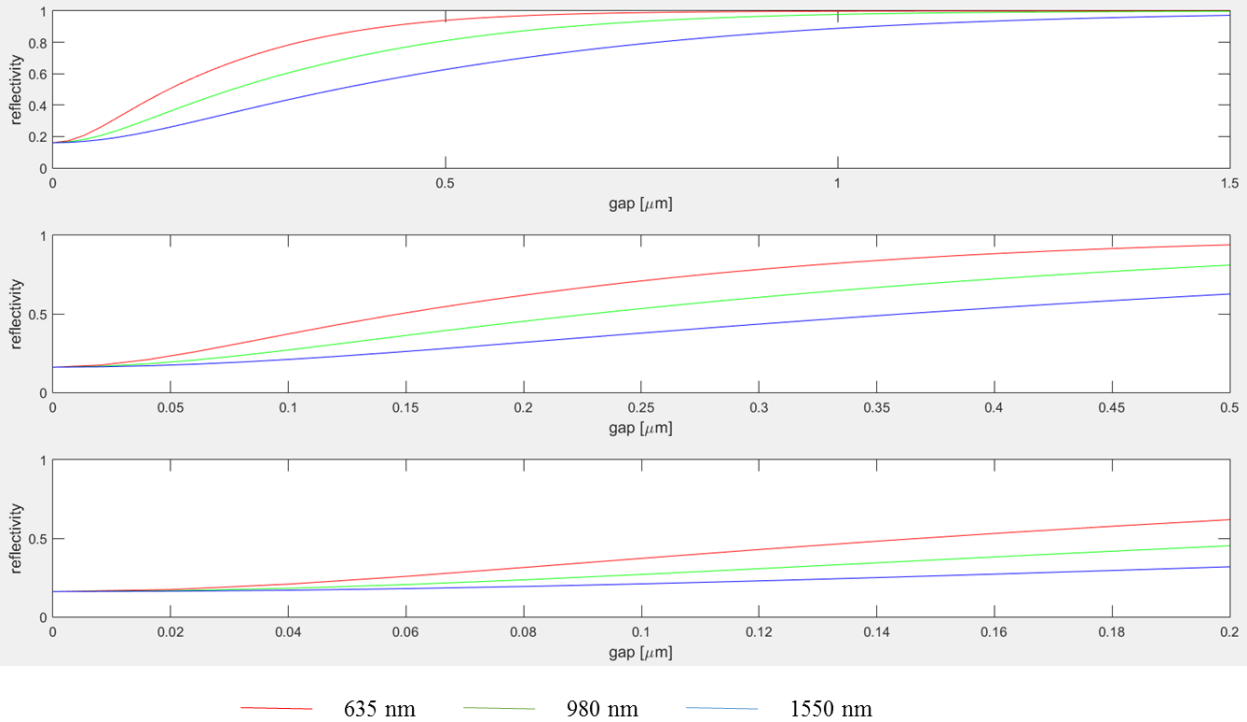

Figure 2-4: Reflectivity at different wavelengths illustrating how reflected beam penetration depth changes with gap. Top shows 0 to 1.5 µm, middle zooms in to show 0 to 0.5 µm, and the bottom further zooms in to 0 to 0.2 µm for a 45°incident beam

Using this code, the reflection versus gap for three different wavelengths were plotted (Figure 2-4). The top plot in the figure is a zoomed out view showing a gap from 0 (touching) to a 1.5 µm gap, and as we see from the plot, if the MEMS interacting structure is more than 1 µm away, then almost 100% of the light is reflected back. The middle plot is zoomed into the 0 to 0.5 µm range and shows that the reflected energy of the 635 nm wavelength is almost 95% at 0.5 µm, but it drops almost to 60% by 1550 nm, which indicates that the chances of detecting a change in reflectivity is much higher at 1550 nm than 635 nm for the same MEMS movement. The final plot is zoomed in from 0 to 0.2 µm to illustrate how the reflectance changes in that nanometer range. So, if we can get scattering structures to 200 nm or closer we should detect change in reflectivity for 635 nm, however there is benefits for using higher wavelengths to produce deeper modulation contrast.

2.2.3 Incidence Angle

As seen from Equation 2.3, the penetration depth of evanescent wave is indirectly proportional to the incidence angle. To understand the effect of incident angle, we plotted the penetration depth (or evanescent wave decay) versus incident angle for three different common semiconductor laser wavelengths (635, 980, and 1550 nm) in Figure 2-5. The critical angle was determined from the refractive index of our working CCR material, BK7 (n = 1.515). From Figure 2-5, we inferred that the penetration depth decreases if the incident angle is not close to the critical angle. If we have MEMS structures at 200 nm from the reflective plane, then for 635 nm wavelength, the incident angle is limited from 41.35° to 44°, which is a short band to target. For 1550 nm wavelengths, the acceptable incident angle range increases to 50° for the same gap. For the purposes of our experiment, we feel we can have incidence beam closer to 43°, after spotting the CCR from camera. However, it will be difficult to target this narrow incident range for other practical applications.

As we learned in Chapter 1, hollow CCRs have high incident (acceptance) angle close to 180°. For TIR-based CCR, the acceptance angle is limited and based on material type, we can either have a CCR made of material with high refractive index (2.1-2.4) to accept broader incident signal. As seen from Figure 2-5 that higher wavelength beams will require fewer CCRs compared to lower wavelength beams, as higher wavelength have higher acceptance angle. Figure 2-6 charts the acceptance angle of the TIR limited CCR device for different CCR glass refractive index values. It illustrates that we will need CCRs made of material with a refractive index in the range of 1.515-2.175 in order to cover incident angles from 40-90°. The number of CCRs required to cover this incident angle range may differ based on the wavelength of the incident beam.

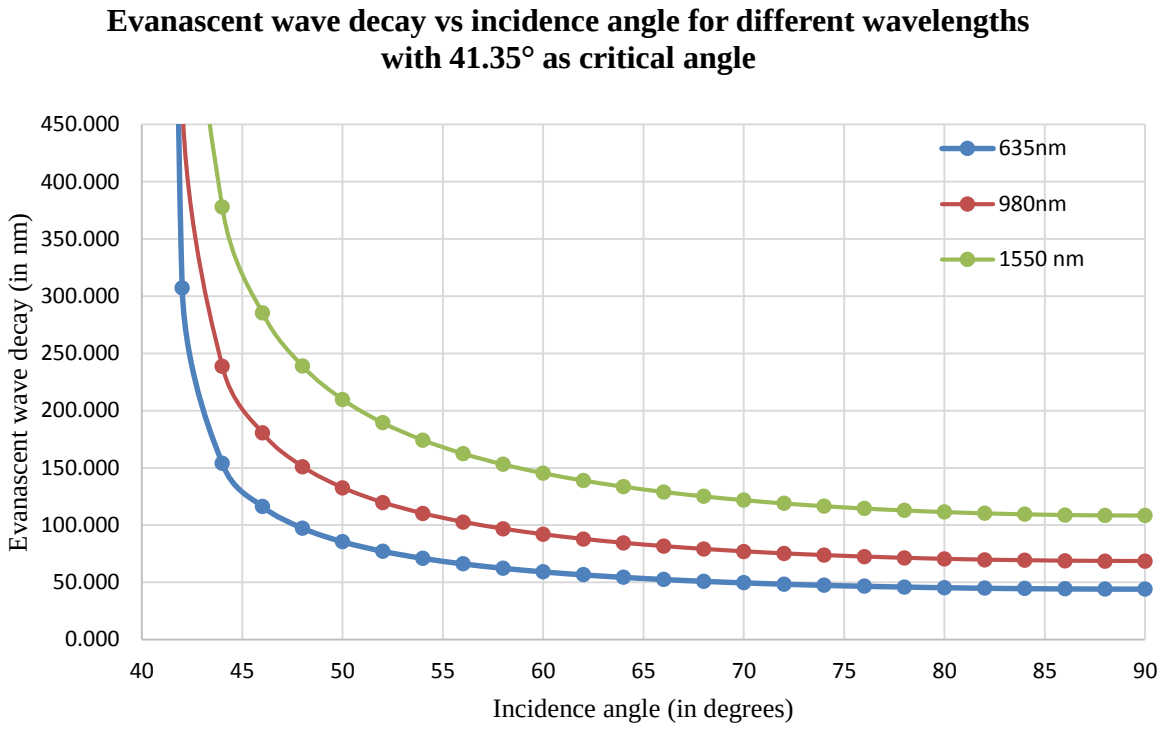

Figure 2-5: Evanescent wave decay vs incidence angle of different wavelengths with 41.35° as critical angle

Until now, we have been discussing incident and acceptance angles as if they were the same. However, TIR-based CCRs have a front face, and the reflecting TIR planes are at an angle, so calculations should compensate for the angle between the TIR plane and the front face. In the commercial CCR if the incident beam is normal to the front face, then it creates an incidence angle of 54.7° at the TIR plane. This incidence angle is higher than critical angle causing the beam to have TIR effect. We also performed calculations using optical coatings consisting of materials with higher refractive indices, either on the front face or mirror face of the CCR and that did not improve the acceptance angle.

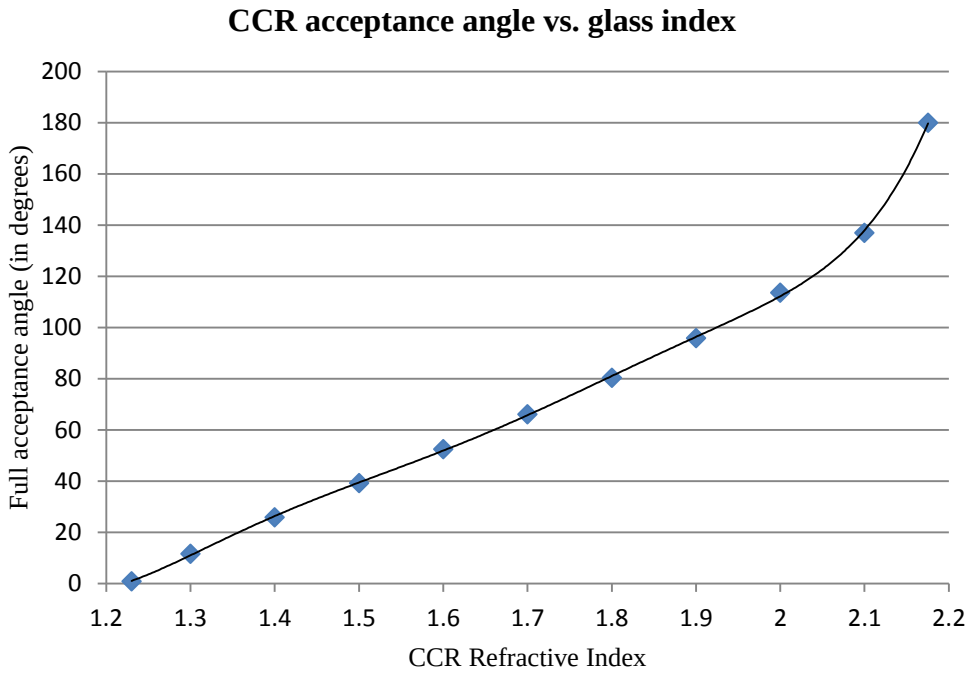

Figure 2-6: Acceptance angle of TIR-based CCR vs. its refractive index

2.2.4 Selection of Commercial CCR

To make the final selection of the TIR CCRs, we looked at various vendor catalogs and discovered that TIR CCRs come in different sizes, angle tolerances, surface flatness, coatings, and other variations. To enable us to make a reasonably-sized MEMS chip that can be attached to the CCR, we chose a 12.7 mm diameter CCR. Several vendors sell similar TIR CCRs with diameter of 7.16 mm, so if we wanted to make our CCR unit smaller, we could. Our selection is made of an uncoated, BK7 material with a λ/8 flatness [12, 13]. Three different variations of angle tolerance were available, 1, 5, and 10 arc-second. We selected the 10 arc-second CCR, as they were inexpensive (less than $20), reasonable for experimental purposes and should allow long range communication. As our process solidified, we considered going to a more accurate 1-arc-second angle tolerance mirror, however they are expensive (~$300/each) and would increase the cost of the transmitter[12, 13]. Our final decision was to order an uncoated, 12.7 mm

diameter, BK7 material, λ/8 flatness, 10 arc-second angle tolerance CCR, and this is what we used for the experiments.

2.3 Requirements for the Receiver Unit

One of the most difficult tasks on the receiver end is to collect enough of the retroreflected signal since at long ranges even a slight misalignment of the CCR mirrors means that we need a large lens to collect all the signal. Even though we collimate the laser beam, there is still some beam divergence (0.5 mrad), which means that the beam at the CCR instead of a dot is like a spot. The spot size of the beam at the CCR can be calculated, and, depending on the misalignment in the CCR mirrors, the retroreflected beam size at different ranges can also be calculated. Using a laser source (λ) of 635 nm and a CCR diameter (*d*) of 12. 7 mm, beam divergence (Θ) was calculated by Equation 2.5, where *w* is the radius of the beam at its narrowest point (also called the beam waist) and given by Equation 2.6 [40].

$$\Theta = \lambda/\pi \mathrm{w} \tag{2.5}$$

$$w = d/2 \tag{2.6}$$

Since the beam divergence is the half angle representation, the total beam spread will be twice that angle. So, for the given CCR dimensions and communication range, the beam spread at the CCR is 6.37e-5 radians (13.13 arc-seconds). This means that if we want to see the spot at the receiver due to just the beam spread at the CCR for a given distance (*d*), then the spot size at the receiver due to CCR beam spread is given by *s*

$$s = \sqrt{w^2 + (\Theta d)^2} \tag{2.7}$$

Also, since there is an offset on the spot size due to misalignment in the CCR during bonding (presently around 30 arc-seconds in our final system and denoted by δ), the offset of the spot size at the receiver due to this misalignment is given by *m*

$$m = \sqrt{w^2 + (\delta d)^2} \tag{2.8}$$

This means we need a lens at the receiver that is large enough to collect all the optical light from the spot size and the offset, a diameter given by a

$$a = s + m \tag{2.9}$$

To enable the receiver system to be portable, we need to ensure that the collecting lens is of manageable size. From above, we understand that the misalignment of mirror plays an important role deciding the size of the collimating lens on the reflector, which would decide if the receiver is portable or not.

Table 2-1: Beam spot at the receiver after beam divergence 0.5mrad (100 arc second) and misalignment 30 arc second (0.15 mrad) due to CCR at different ranges

CCR range (km)	Spot size @ receiver (mm)	Offset due to CCR misalignment (mm)	Spot size + offset (mm)
0	12.7	0.0	12.7
0.1	14.2	14.5	28.8
0.2	18.0	29.1	47.1
0.4	28.5	58.2	86.6
0.5	34.3	72.7	107.0
0.6	40.3	87.3	127.5
0.7	46.3	101.8	148.1
0.8	52.5	116.4	168.8
0.9	58.7	130.9	189.6
1	64.9	145.4	210.4
1.1	71.2	160.0	231.2
1.2	77.4	174.5	252.0
1.3	83.7	189.1	272.8
1.4	90.0	203.6	293.6
1.5	96.3	218.2	314.5
1.6	102.6	232.7	335.4
1.7	109.0	247.3	356.2
1.8	115.3	261.8	377.1
1.9	121.6	276.3	398.0
2	128.0	290.9	418.8

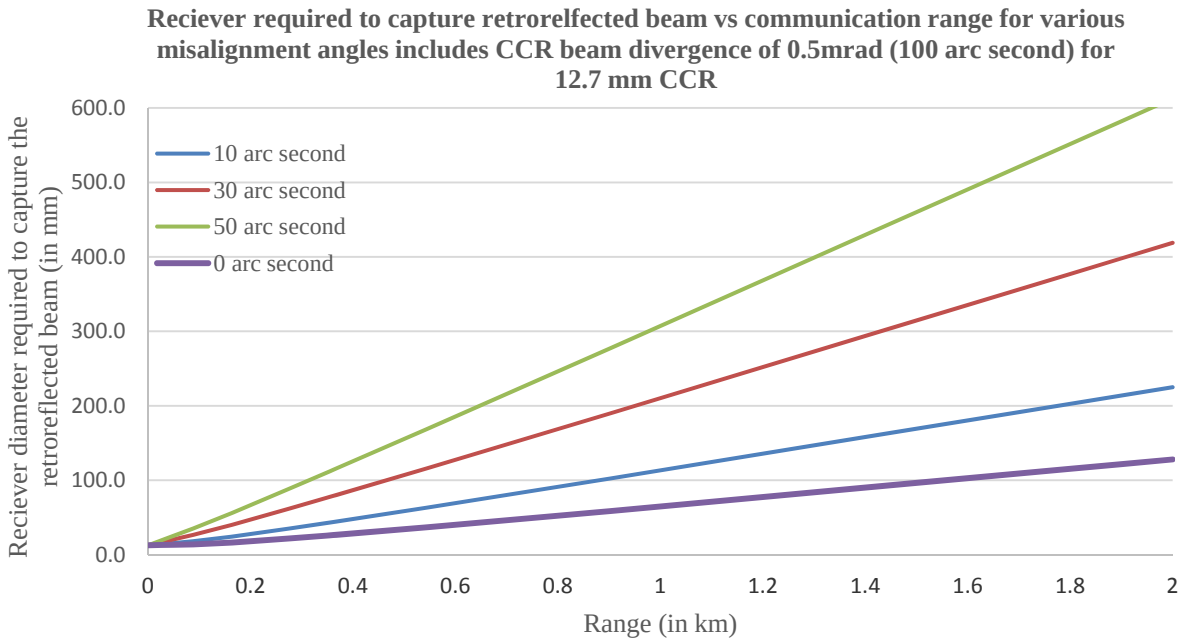

Figure 2-7: Receiver size required vs communication range at different misalignment angles

As seen in Table 2-1, when the CCR mirrors are misaligned by 30 arc-seconds, a 210 mm diameter collecting lens is required to capture the retroreflected signal. We see in Figure 2-7 how having 0 – 50 arc second misalignment of mirrors effected the beam spot deviation for a 12.7 mm CCR, if we have 50 arc-second misalignment on the mirrors, then the required collecting lens on the receiver end needs to be more than 600 mm in diameter for a 2 km optical communication range. The benchtop initial design and improvement of the receiver unit is discussed in Chapter 5.

2.4 Requirements of the MEMS Chip

We selected a BK7 (n=1.51 for 635 nm) [43] 12.7 mm, uncoated, TIR-based commercial CCR. The CCR has a 12.7 mm long front face where the light comes in, and three orthogonal sides on which the beam totally internally reflects before finally emerging from the front face parallel to the incident beam. As seen in Figure 2-8, all three orthogonal sides measure 7.77 mm from the vertex to the top of the side, and the two ends of the flat sides are connected by an arc

as shown in Figure 2-8. This meant that there was an approximate 7.77 x 7.77 mm active area on the CCR where we wanted our MEMS structures to interact with the evanescent waves during TIR. Dimensionally, we wanted a silicon on insulator (SOI) chip larger than 7.77 mm on one side to enable access to the electrostatic electrodes. We decided the dimension of the MEMS die would be 10 x 8 mm, which would give us an additional 2 mm area to place the electrode bond pads.

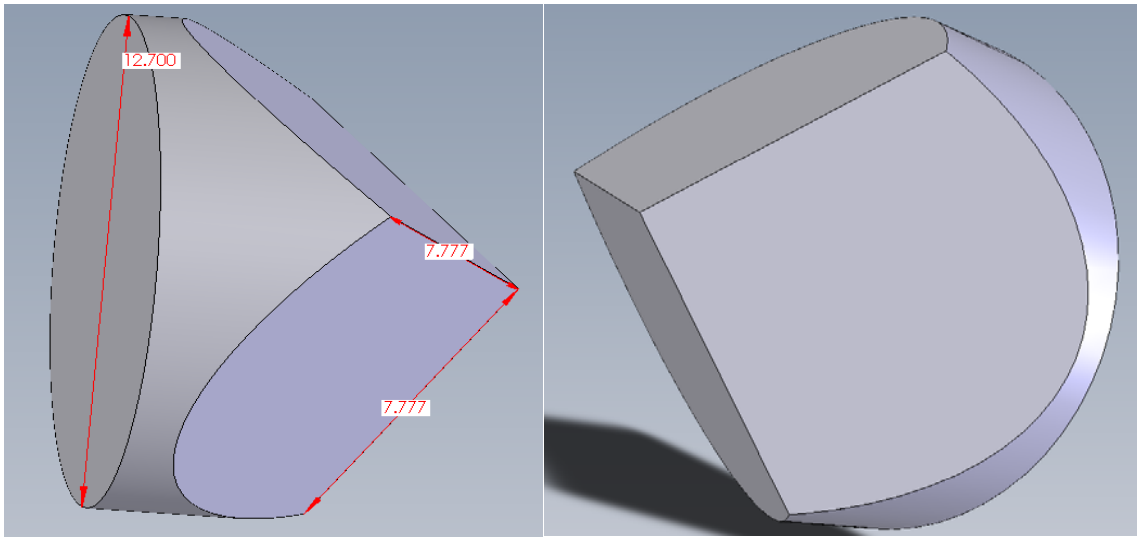

Figure 2-8: 3D model of the CCR illustrating the height and other dimensions [12]

We would like to use as little power as feasible to actuate the MEMS structures and meet the electrical requirements for the MEMS chip. We decide to use ½ AA (3.V) battery to power the transmitter unit, so we wanted to ensure that we can actuate the MEMS structures in 3-15 V range, using battery or commonly available compact DC-DC converters. The ability to move the MEMS structure in and out of plane would allow us higher contrast modulation, which meant that we wanted to have three electrodes and move the structure either in or out of plane. Additionally, a structure modulation frequency of ~ 1-10 kHz was desirable for high data rate, running them higher than that using the same actuation voltage will be worthwhile. In the next section we perform pull-in calculations for different styles of MEMS structures using this

information, and then compute the energy consumption per bit for our transmitter and compare it to existing, solely MEMS mirror-based CCR systems.

2.4.1 MEMS Electrostatic Structures

There are several actuation methods available. For our application we needed an actuation method that had low power consumption, operated at a moderate-high frequency, was inexpensive to fabricate, and was unaffected during the bonding of the glass lid. We examined electrostatic, thermal, piezoelectric, magnetic, and other actuation methods, and determined that electrostatic actuation methods seemed to meet all the above criteria [44-46]. This, combined with our previous experience fabricating structures that use electrostatic actuation and limited resources and budget, led us to choose the electrostatic modulation method to actuate our structures. This concept is shown in Figure 2-9, in this method a mechanical spring is connected to one of the parallel plates. When potential is applied, the moveable parallel plate has electrostatic force that opposes the restoring force of the spring and moves towards the other plate.

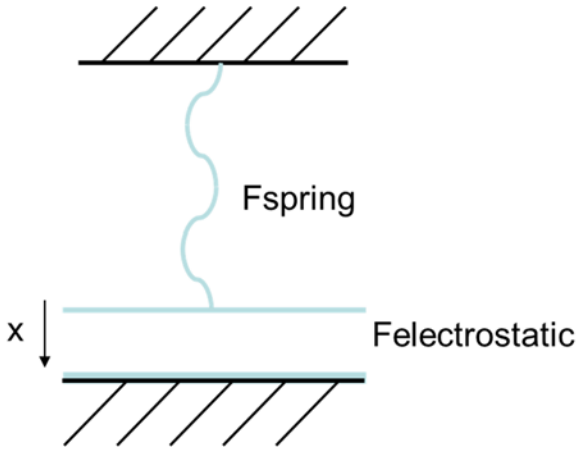

Figure 2-9: An electrostatic actuator schematic with a spring connected to one of the parallel plates of capacitor. When pulled in, enough electrostatic force generated to overcome the spring's restoring force.

The force required to pull *n* springs by *x* distance is given by Equation 2.10, where *k* is the spring constant. The distance *x* is determined by the gap (also referred as sacrificial gap) between the parallel plate. If the sacrificial gap is *g* then the pull-in gap required (*x*) is one third the gap [35, 45, 47], as shown by Equation 2.11.

$$F_{spring} = nkx \tag{2.10}$$

$$x = g/3 \tag{2.11}$$

Assuming that the springs are directly connected to the parallel plate in a straight line (also referred as straight tether format), the value of the spring constant *k* is given by Equation 2.12 [45, 47]. To improve accuracy, a detailed finite element analysis (FEA) of the spring needs to be performed. Equation 2.12 also uses the variables $E_{silicon}$ (the Young's modulus of silicon), and *w*, *t*, and *l* (the width, thickness and length of the spring); we have added suffixes to each of these so that we do not confuse the spring and parallel plate variables.

$$k = E_{Silicon} w_{spring} t_{spring}^3 / l_{spring}^3 \tag{2.12}$$

The counter-electrostatic force is given by Equation 2.13 [electrostatic], where ε_o is the permittivity of free space, l_{plate} and w_{plate} are the length and width of the parallel plate, *V* is voltage applied, and *d* is the gap between the parallel plates.

$$F_{electrostatic} = \frac{\varepsilon_o l_{plate} w_{plate} V^2}{2d^2} \tag{2.13}$$

When the parallel plates are pulled in, the spring is elongated by one third, and the parallel plate gap is two thirds its original gap with no voltage applied, so from Equations 2.10, 2.12, and 2.13, we get the pull-in voltage shown by Equation 2.14 [37, 44, 46]

$$V_{Pull-in} = \sqrt{\frac{8\, n E_{Silicon} w_{spring} t_{spring}^3\, g^3}{27\, \varepsilon_o l_{plate} w_{plate} l_{spring}^3}} \tag{2.14}$$

We used Equation 2.14 to guide our design calculate the pull-in voltage for the different variants we intended to include in our mask design. We started with a 100 x 100 µm plate design and a spring with a width of 6 µm, a thickness of 3 µm, and length of 200 µm. Using four of these springs and a sacrificial gap of 3 µm, we got a pull-in voltage of 18.6 V. Similarly configured 200 x 200 µm and 500 x 500 µm plates gave reduced pull-in voltages of 9.3 V and 3.72 V respectively. We did not want to change a lot of variables, so, keeping the spring thickness (3 µm), gap (3 µm) and width (6 µm) constant, we altered the plate size, spring length, and number of springs to get structures with a wide range of pull-in voltages (Table 2-2). We used three different spring styles: short spring, long spring, and meander spring. All springs 200 µm and longer were of the meander type. It is important to note that these pull-in voltages illustrated in Table 2-2 are in plane, i.e. structure silicon moving towards the substrate silicon, however the gap between the glass and the MEMS structure will be in nm-range from Equation 2.14 and the pull-in voltage will be expected lower than this.

Along with the pull in voltages we also calculated the resonance frequency of the MEMS devices using Equation 2.15 [45]. The resonance frequency data will guide us as to what the optical communication data rates will be. The value of spring constant of an individual spring (k) was already available from Equation 2.12, to calculate the effective or complete spring constant we take the product of number of springs (n) and the spring constant of individual spring. To calculate the mass (m) of the plate, we calculated the area of MEMS plate and subtracted the area of release holes. The resonance frequency for each plate is also tabulated in Table 2-2 along with pull in voltages.

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k_{total}}{m_{plate}}} \tag{2.15}$$

Table 2-2: Variation of MEMS structures along with their calculated pull-in voltages and resonance frequency

Plate size (in µm)	Spring length (in µm)	Number of springs	Calculated pull in voltage (in V)	Resonance frequency (in kHz)
100x100	200	4	10.14	7.12
200x200	55	4	35.18	24.69
200x200	150	4	7.81	5.48
200x200	200	4	5.07	3.56
500x500	450	4	0.6	0.42
500x500	250	4	1.45	1.02
500x500	150	4	3.12	2.19
500x500	150	8	4.42	3.1

Also important to note that in these calculations, bending and tipping effects are not considered, and the spring constant is an approximation, FEA analysis would yield more accurate information. However, these empirical calculations give us guidelines as how one parameter impact the pull-in voltage and resonance frequency, though the exact numbers may be off, however the trend that it shows is accurate. We used the information form these calculations and designed and fabricated the structure that will be discussed in detail in the next chapter.

2.4.2 Calculation of Energy Needed Per Bit

In this section we calculate the energy consumed per bit using our suggested communication method, which will enable us to compare this model with other communication methods and to understand its key merits. In the above designs, the parallel plate moves in and out of plane as each bit is being transmitted. This means we can calculate the energy required per bit by first computing the capacitance of the parallel plate as given by Equation 2.16 [37, 45] and

then determining the energy required to charge the plate. For 200 µm plate, we have an array of 26 row and 26 columns which yields 676 mirrors, the total capacitance of capacitor of mirrors for a gap of 2 µm is 119.65 pF, we can similarly calculate the capacitance for the anchor area, keeping in mind that there is oxide present as dielectric which will add to the capacitance, upon calculations we get capacitor under anchor area to be 68.69 pF, so the total capacitance of mirror plus anchor area sums up to be 188.34 pF.

$$C = \varepsilon_o A_{plate}/g \tag{2.16}$$

$$I = \frac{dQ}{dt} = C\frac{dV}{dt} \tag{2.17}$$

The current consumed to charge this capacitance is given by Equation 2.17, where approximately the capacitance remains constant, we can write the current consumed in terms of *C* and *V*. If we take a design with a pull-in voltage of 6 V operating at 10 kHz, then the current consumption to modulate that capacitance is 11.3 µA, which would consume 67 µW to modulate the MEMS structure. We calculated that it would require 6.78 nJ/bit, or 67 µW at 10 kHz of energy, to transmit one bit of data, which is extremely low power. However, this indication of low power consumption during communication is sufficient reason to pursue the technology.

2.5 System Parameter

Earlier we performed calculations to understand the properties of evanescent wave decay and MEMS structures, which helped us design the transmitter. For the receiver we calculated the size of a collimating lens required to collect the retroreflected signal as a function of communication range, misalignment of mirrors, and beam divergence for the selected 12.7 mm diameter CCR. Two other important aspects of the receiver were to calculate the retroreflected signal power at the receiver and the optical detector signal-to-noise ratio (S/N) to the incoming retroreflected signal.

To compute the retroreflected power from the CCR, we first need to analyze the power incident on the CCR, for that we use Equation 2.18 [2, 15, 38], where *P* represents the power (the suffix below that to provide more description), *A* is the area, T_{atm} is the transmission of light due to atmospheric effect, from [48] we inferred that it is 0.85 at 1 km. $R_{mirror\ reflectivity}$ is the reflectivity from the mirrors, and from literature it is 0.96 [15, 38]. For the selected 5 mW laser 635 nm (red) laser with a beam divergence of 0.5 mrad, and using Equation 2.1 for 1 km, the incident spot size or beam diameter was 500 mm. Using the above information and Equation 2.18, we computed that 2.63 µW of power is incident on the CCR. Once we knew the power on the CCR, we used Equation 2.19 to calculate the retroreflected power at the receiver. A collimating lens with a diameter of 150 mm was selected and the beam spot size (or diameter) was calculated with a beam divergence (0.5 mrad) and misalignment (30 arc second) of the CCR. From equation 2.19, we computed that at 1 km for the parameters selected above, 1.14 µW of power is retroreflected and collected by the receiver and incident of the detector.

$$P_{CCR} = P_{laser} \frac{A_{CCR}}{A_{incident\ spot}} T_{atm} R_{mirror\ reflectivity} \tag{2.18}$$

$$P_{reftroreflected} = P_{CCR} \frac{A_{collimating\ lens}}{A_{CCR\ beam}} T_{atm} \tag{2.19}$$

To filter out the retroreflected signal from other light sources, we used a narrow band-pass filter. We can use micrometers (or experiment) to set the detector position, so that the collected light focuses on the detector. We can either use a detector with pre-amplifier or a normal response detector with an external preamplifier circuit to get the received optical signal in measurable electrical levels. To understand the difference in S/N of the above two mentioned detectors, we selected two detectors from Edmund Optics, 59-391 and 57-507, for calculations. The 59-391 detector is a silicon photodiode with built-in preamplifier; the 57-507 is a normal

response silicon photodiode. Both detectors have an active area of 0.8 mm^2. Detector 59-391 has a sensitivity of 13.5 mV/µW for 635 nm [12] and noise equivalent power (NEP) of 25 nV/√Hz. So when 1.14 µW of reflected power is incident, a 15.36 mV signal should be produced at the detector. The actual signal is the modulated retroreflected signal, considering 10% modulation, the true signal works out to be 1.5 mV. For the entire optical signal coming in there is shot noise and dark current noise, we believe other noise levels will be low and are presently ignored. Using equation 2.20 [49], where *q* is the elementary charge of an electron, *I* is photo induced current and *f* is the frequency bandwidth, we calculated the shot noise to be 0.0314 nA, for a 500 ohm load (from datasheet); the equivalent voltage is 15.67 nV.

$$Shot\ Noise = \sqrt{2qIf} \tag{2.20}$$

The noise equivalent power of the detector at bandwidth frequency (100 kHz) upon calculation works out to be 7.91 µV. Since the NEP of the detector (including amplifier and dark current noise) was way higher than shot noise, the resultant RMS noise for the detector was same as 7.91 µV at 1 km. Using this value we calculated the S/N to be 194 (or 45 dB) for this detector, this S/N is suitable for this application and this detector can be used for detecting retroreflective power from CCR.

For the normal response silicon detector (57-507), the responsivity is 0.4 A/W for 635 nm with a NEP of 6.2 fW/√Hz, considering 100 kHz bandwidth, the dark current noise was calculated to be 0.78 pA. For 1.14 µW incident on the detector, a signal of 0.455 µA will be produced, resulting in a shot noise of 0.1207 pA from Equation 2.20. Equivalent noise is the RMS of shot noise and dark current noise, which computes to 0.7934 pA. Considering 10% modulation, the retroreflected signal is 45.5 nA, which gives us S/N of 57349 (95 dB). The S/N of the normal response detector is 295 times higher than the amplified detector at 1 km range; for

a range of 0.01 km it is 30 times higher. Using the normal response detector, we need to ensure that the amplifier circuit design has low noise, so that it is advantageous to use that detector.

From these calculations we performed, we feel that the modulated retroreflected signal to optical noise ratios are promising for 1-km communication for the system.

2.6 Conclusion

In this chapter, we presented a commercial CCR-traditional MEMS hybrid concept based on the scattering of evanescent waves. We selected a 12.7 mm, uncoated, BK7, 10 arc-second misaligned reflector for our experiment. We acknowledge that smaller and more accurate reflectors are available, however, we thought it prudent to make our selection with an eye to expense. We performed calculations and inferred that having an array of CCRs made of material with varying higher refractive index will help us achieve wider acceptance angle. We also noted that as wavelength increases, we get better penetration depth and a wider angle of acceptance, however, since our available and convenient to view equipment works at 635 nm (red), we used 635 nm as our source wavelength. We also discussed the requirements for the retroreflected signal receiver, did empirical calculations on the transmitter side to figure out designs for the MEMS structure and spring, and calculated the approximate energy consumption per bit for the transmitter (CCR only). In the next chapter, we will further discuss the design and fabrication of the MEMS chip.

CHAPTER 3

DESIGN AND FABRICATION OF THE MEMS CHIP

In the previous chapter, we were able to perform empirical calculations and understand the optical and actuator parameters needed to develop an optical communication system that would allow us to interact with the evanescent waves of the retroreflector. This chapter[7] discusses in depth the process development, design of structures, and finally, fabrication of the designed structures through the developed process to achieve a MEMS chip that is able to bond to the commercial CCR. This MEMS chip will have electrodes which will enable the electrostatically modulated micro structures to interact with evanescent waves and disrupt them.

3.1 Development of the Process

In the MEMS chip we knew that we required silicon modulating array like structures, however how is that structure going to be bonded to the CCR was undefined. Also how are we going to get the MEMS structure close to the TIR plane? To solve this, we created a two wafer approach where the MEMS modulating structures will be fabricated on silicon wafer and bonded to a glass lid and that lid will be bonded to the CCR, thus shifting the TIR plane to near the MEMS modulating structures. Now if the glass had transparent conductive film like indium tin oxide (ITO) [50-52], the moveable structures can be modulated both toward the silicon as well as closer to the TIR plane. To chalk down an exact process we first laid out the goals for the glass lid:

[7] Part of this Chapter was published in IEEE Journal of Micro Electro Mechanical System , 2015, DOI: (10.1109/JMEMS.2015.2428275) and permission to use is included in Appendix A

a. Have a transparent and conductive electrode like Indium Tin Oxide (ITO).
b. Have a gap of about 200 nm between the ITO electrode on the glass lid and the MEMS structure that meant we needed to indent other areas of glass lid to produce a gap of 200 nm, when using a bond material.
c. Create the glass lid bond area, which goes around the structures, and bond the ITO electrode on the glass lid to the ITO electrode on the SOI chip using previously developed Au-Au thermal compression bonding.
d. Ensure that the size of the glass lid is smaller than the SOI chip so that we can wire bond to the electrodes on the SOI chip.
e. Ensure the ITO electrode can be easily addressed along with MMES modulator electrodes.

To achieve the above chip functionality, we designed three masks and a process flow to fabricate the structure (cross-section steps are shown in Figure 3-1). About the MEMS structures, from earlier project, we had experience in fabricating structures and electrodes for electrostatic actuation using single-sided polished silicon wafers and surface micromachining process. The wafers used were inexpensive, however, a lot of effort was spent in tuning the intrinsic stress of the films. Apart from that fabrication process, using single-sided polished silicon was complex and requires exact alignments [45, 53, 54]. Learning from that experience, this time we invested into silicon on insulator (SOI) wafers that use single-crystal silicon as the structure layer, followed by a sacrificial oxide layer and then the substrate silicon. This made the fabrication simpler and saved time as we did not have to tune for the intrinsic stress in the moveable plates film. For the MEMS structures we needed electrostatic structures and metal to probe the electrode as we planned on using structure and substrate silicon as electrodes.

Considering all the above, we developed the process flow illustrated in Figure 3-1, which shows a cross-sectional view of a glass wafer (on left) and an SOI wafer (on right). The steps of the cross-section are shown in (a) – (d) and then both the components were bonded in the bottom figure. In glass wafer steps (a) – (d), a die was arrayed on the wafer. SOI section steps (a) and (b) show individual element cross-sections (which are a small part in the die/chip) and steps (c) and (d) are chip-level cross-sections. Finally, both the die-level chips are mated and bonded together.

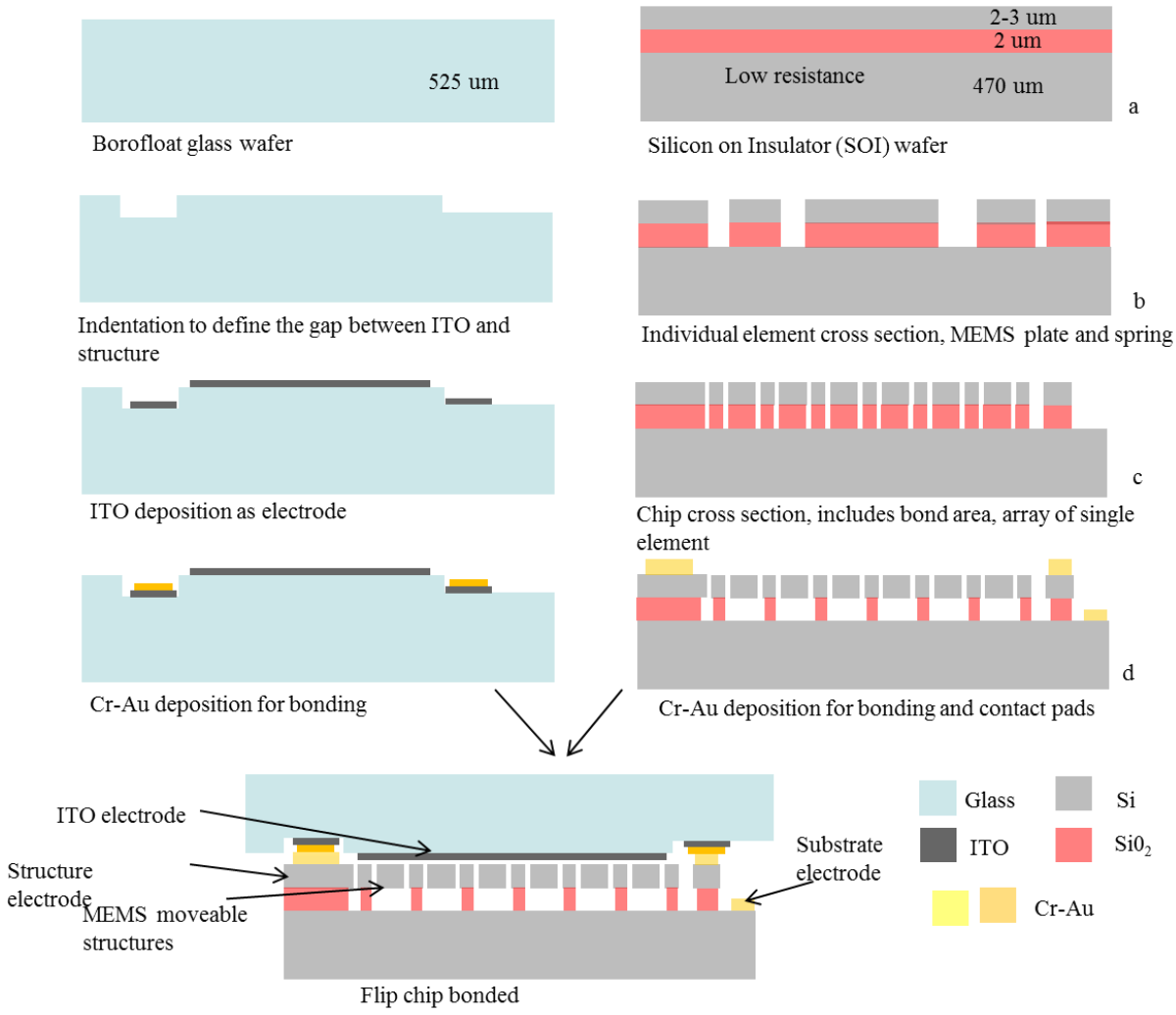

Figure 3-1: Cross section view of the glass and SOI wafer. Steps (a) and (b) on the SOI wafer are wafer-level fabrication and steps (c) and (d) illustrate chip-level fabrication.

3.2 Design of Structures and Electrodes

The TIR CCR has three flat mirrors and each face of the CCR mirror has two straight lines connected by a circular arc (see Figure 2.8). While designing the MEMS plates that interact with the TIR mirror, we would have liked to maximize the TIR mirror area. However, it will be difficult to have a chip with an arc on one end. We know that the two sides of the mirror are 7.77 x 7.77 mm from measurements taken of the faces of the CCR (Chapter 2). To ensure that the MEMS chip covers most of the active area of the CCR and still provides access to its electrodes, a 10 x 8 mm chip was designed. Considering the bond area and the area needed for plate array, busbar and routing, we had the modulators covering a somewhat smaller than optimal 6.5 x 6.5 mm area. A 9 x 8 mm indium tin oxide (ITO)-coated glass lid chip was used to protect the MEMS structures during assembly and operation, to set the structure-glass gap, and to allow electrostatic actuation of the silicon plate elements toward this glass lid. The glass lid was thermo-compression bonded to the SOI MEMS chip and this assembly was bonded to the CCR using a UV-cured epoxy. Three electrode bond pads were provided that attach to the MEMS substrate, the movable plates, and the ITO-coated glass lid. The electrodes were located in an exposed 1 x 8 mm area of the bonded SOI-CCR chip assembly. Test structures were also designed and placed in the empty 1 x 8 mm exposed area on the SOI chip. This test area allows us to test different structures of plates with different spring configurations.

The overall mask layout is shown in Figure 3-2. Each mask is labeled with its name and features. Additionally, there is a coarse visual alignment mark (the large triangle-like structure) and fine alignment marks next to the coarse alignment mark. We also selected eight different variations of MEMS plate and spring combinations. We get nine instances on a wafer for each variation, as seen in the mask layout. The mask layout shown in Figure 3-2 is based on two-

wafer SOI and glass wafer fabrication. The details of mask design for each wafer are described below.

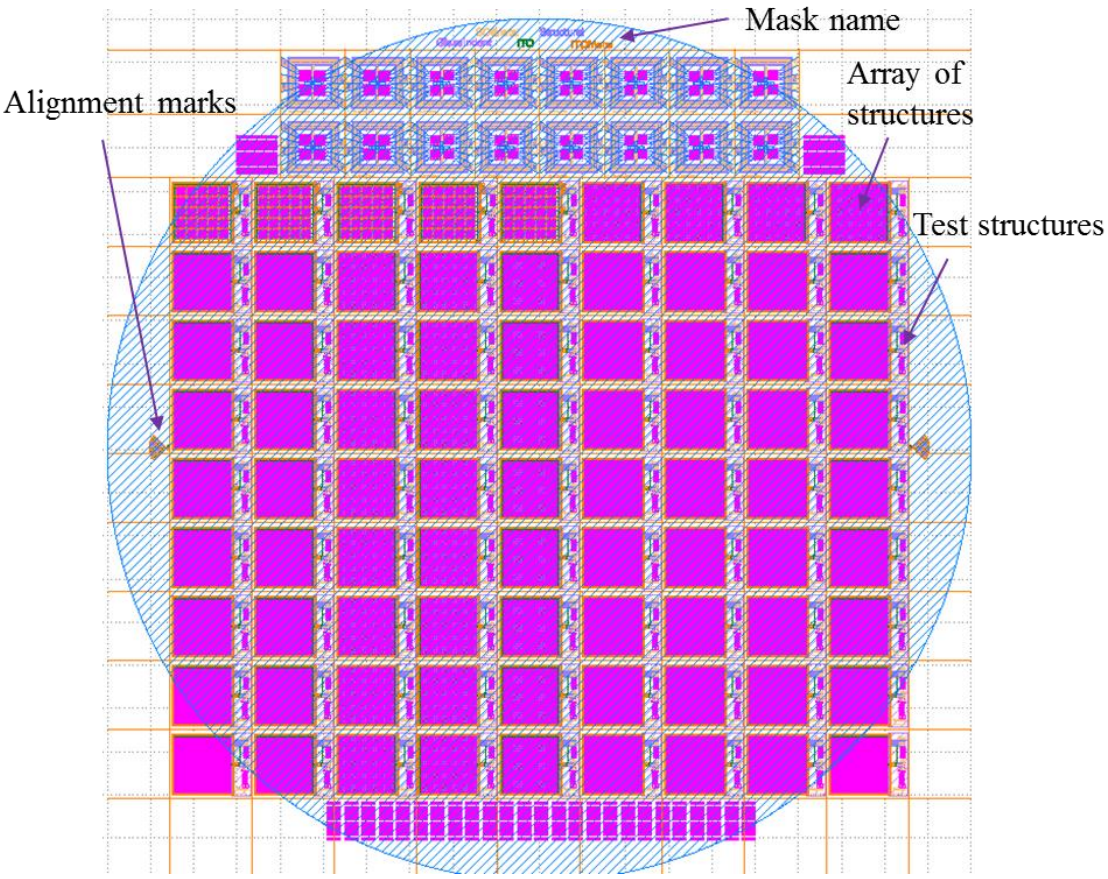

Figure 3-2: Overall view of both SOI and glass mask design

3.2.1 Silicon on Insulator (SOI)

The SOI wafer has two masks: *structure* and *structure metal*. To enable ease in design, we also laid out a third layer, *release holes*, that was cut out of the *structure* mask. During development of the mask, the fab house combines the *structure* and *release holes* CAD masks into a single mask.

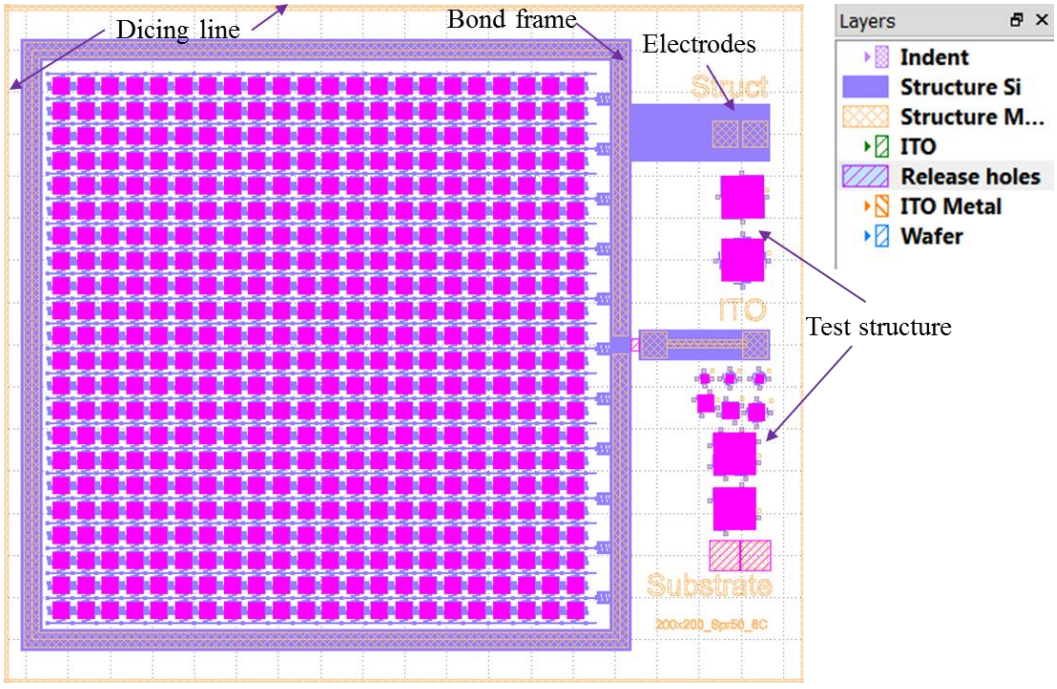

Figure 3-3: 200 x 200 µm MEMS plate array with layers

A chip level view of one of the chips on the mask is shown in Figure 3-3. Except for the active area, which contains the MEMS plate and the spring, the frame work was similar for all the chips. The *structure* mask defines the movable structures, springs, anchors, and the bond frame that mates with a glass lid chip (discussed next). The mask consists of chips with arrays of MEMS plates that vary in size (100x100, 200x200, and 500x500 µm) and having different spring geometries. The active area was surrounded by a 260 µm-wide bond frame area. A 3D model of one of the MEMS structure (500 x500 µm plate) without release holes and test structures is rendered in Figure 3-4 to illustrate the vision behind the structure design.

The holes designed to release the plate and allow the spring area to move in and out of plane are 3 x 3 μm^2 with a pitch of 9 µm. These are provided to etch away the buried oxide under the plate and release the structure, and to provide scattering features for the evanescent waves. The anchor areas were designed without release holes and are wider (20 µm) so that they do not fully release during the buried oxide etching step.

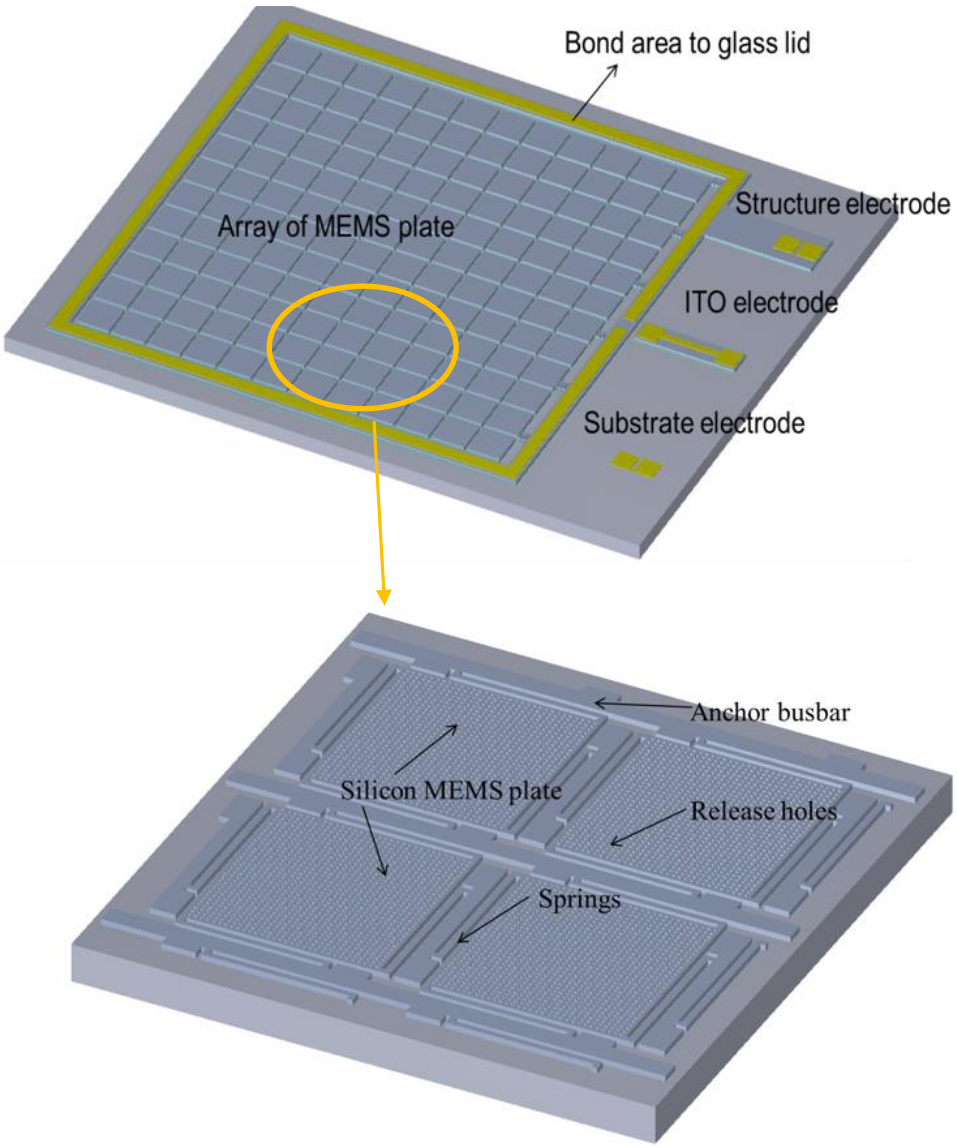

Figure 3-4: Top is a 3D solid model developed in SoftMEMS illustrating the electrodes and MEMS array. Bottom shows a zoomed-in view of springs, release holes and busbar.

The structures are arrayed in the active area depending on their size (for instance, for a 100x100 µm plate design, 34 rows and 35 columns of features were placed in the active area). Two rows shared a common bus, which was connected via-high resistance connections to the wire bonding pad. The high-resistance traces and row busbar were included so that if one, or a few, of the plates within the array were electrically shorted to the substrate or ITO, the entire array of plates would not stop functioning.

Using simple resistivity calculations, we calculated for a thickness of 2 µm of 1 ohm-cm resistivity structure silicon; the resistance from electrode to the last row of plates was a sum of the resistance of five fuses, the busbar, and the springs. The total resistance from the bond pad to the plate was 3.41 Mohm per row. The anchors were designed so that after the release step there was still a substantial amount of silicon dioxide (almost half) under the anchor area. For the 500 x 500 µm plate, the capacitance of a row of devices was calculated to be 17.08 pF with an electrical RC cut off frequency [45] of 17.17 kHz. The capacitance per row for a 200 x 200 µm and 100 x 100 µm plates was 7.53 pF and 4.37 pF, respectively, and the cut off frequencies were 38.93 kHz and 67.07 kHz. The capacitive effect of oxide under the anchor area was significantly higher for a 100 µm plate than for the 500 µm ones; considering the mirror, anchor, and spring areas, the larger plates have a fill factor of 85%, as opposed to the 200 µm and 100 µm plates, which have fill factors of 64% and 29% respectively.

The *structure metal* mask defines lid and wire-bond metal areas (Cr/Au). The metal area for the lid on the structure silicon has a clearance of 40 µm on each side. As mentioned above, the structure silicon and the gold bond area has a width of 260 µm and 180 µm respectively. On the wire bond metal area the structure and substrate electrodes are on their respective silicon areas, however an isolated electrode was designed for the ITO and that particular isolated area mates with the glass lid once bonded to provide access to ITO electrode.

The area on the chip, where we have test structures as shown in Figure 3-3 consist of single instances of the MEMS plates, six of the eight plates are located in the area between substrate and ITO electrode and the other two between ITO electrode and structure electrode. Every chip has the test structure so all the structures on any chip can be tested. A 3D rendering of one of the 100 µm MEMS plate test structures after the release fabrication test is shown in Figure

3-5. One of the things visible in the Figure 3-5 rendering is the leftover oxide under the anchor area, similarly oxide also remains underneath the electrode and bond frame Figure 3-4, but it is not easily seen in the rendering due to the small thickness of oxide and the fact that it is under-the substrate silicon edges.

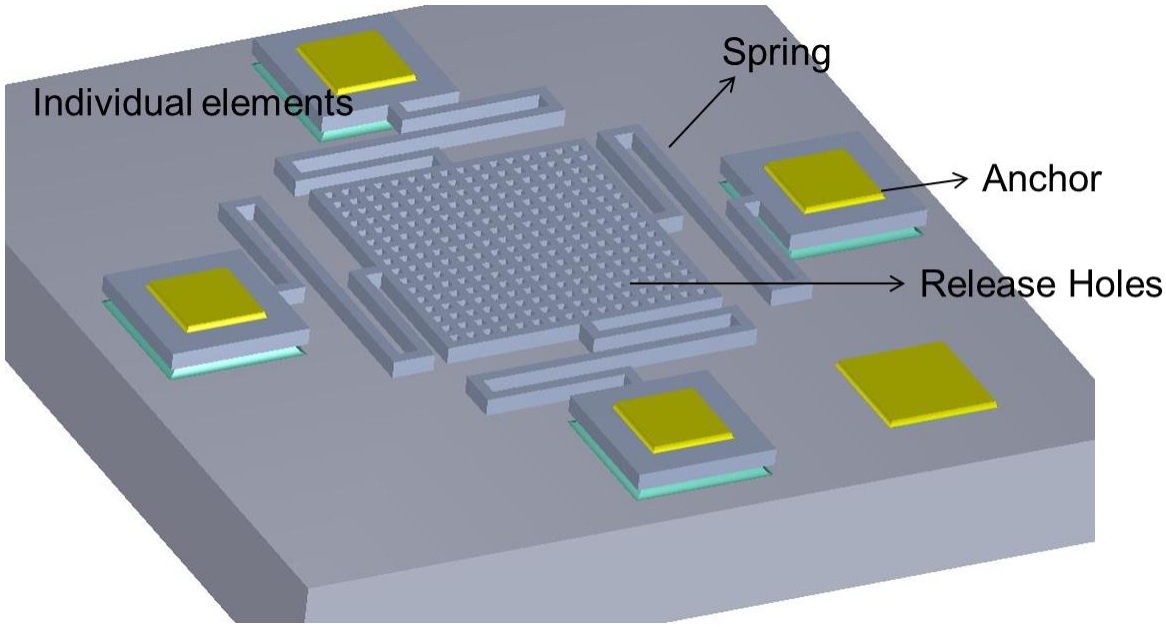

Figure 3-5: 3D rendering of a 100 x 100 µm MEMS plate after release illustrating that the oxide (green) is removed under MEMS plate and springs but not the anchor area

3.2.2 Glass Wafer

The glass lid wafer was patterned using three masks: *indent*, *ITO* and *ITO metal*. The *indent* mask provides an indentation in the glass under the bonding area and defines a desired gap between the SOI structure and ITO once the glass and SOI chips are bonded. Indentation is done in the bonding region, which is near all four edges of the chip. The indent depth in the glass was designed as the sum of the two bond metal layers minus the desired gap between the movable structures and ITO. Though ITO metal is present in the bond area, it is also present on the glass to make the ITO electrode, so the ITO thickness does not affect the depth of

indentation. A 2D layout of the mask is shown in Figure 3-6 and the 3D rendering of the glass lid chip is shown in Figure 3-7.

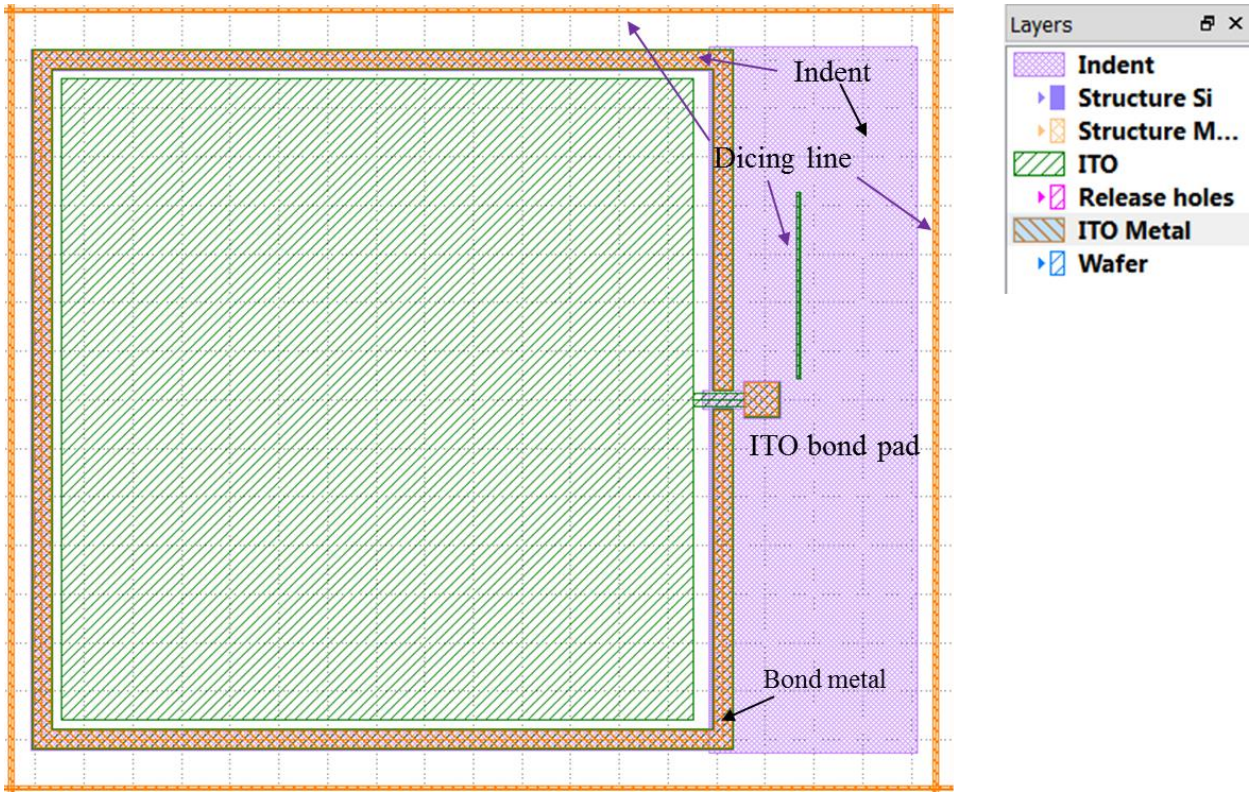

Figure 3-6: 2D image of a glass lid

Following this is the *ITO* mask that defines the area where a conductive/transparent ITO layer was deposited. ITO was deposited on the bond area and on the structure area, as shown in Figure 3-6. The bond area ITO and the structure area ITO are electrically isolated, the bond frame goes around however there is a 200 µm disconnect area, where the ITO electrode signal is routed out to a pad which bonds to the SOI wafer via Au-Au thermos-compression bonding and thus allowing access to ITO electrode on glass lid via structure silicon. The minimum feature size for the ITO mask is 25 µm with a spacing of 25 µm; this allows enough leeway if there is any misalignment. A dicing line is drawn on the ITO layer to indicate where the glass lid can be diced so that when it mates with the SOI chip the electrodes on the SOI wafer are accessible.

Finally, the *ITO metal* mask was used to deposit Cr/Au on the bonding areas as shown in Figure 3-6. As seen in the figure, there are dicing lines in the *ITO metal* and *ITO* masks. These are to allow a dice of the glass lid to a size similar to SOI and then a little more so that the electrode areas on this chip were exposed.

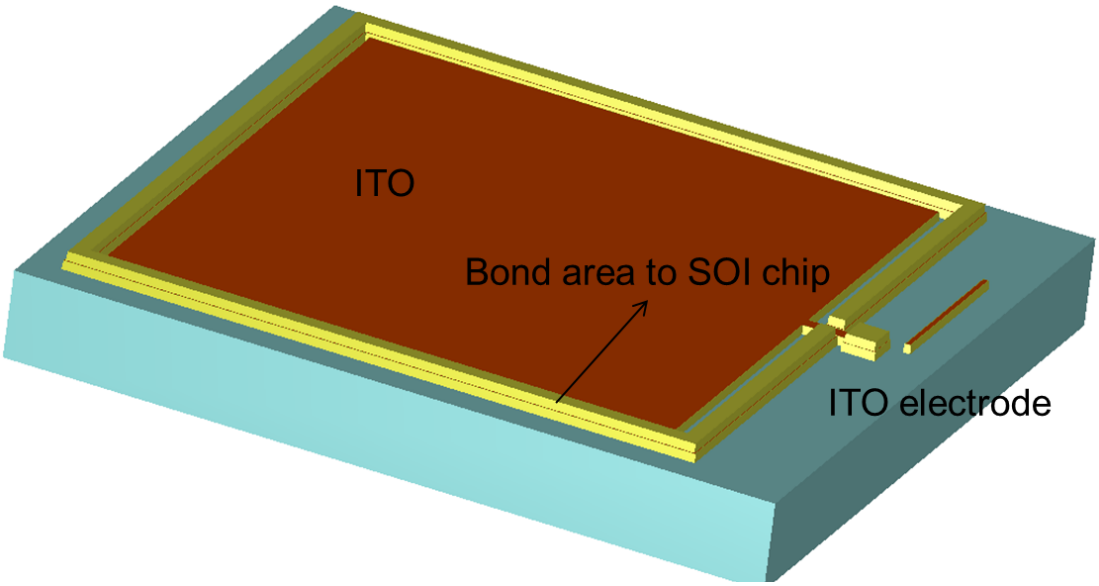

Figure 3-7: Glass chip design for bonding a conductive glass lid within a few nm of the MEMS SOI chip

3.3 Fabrication of MEMS Chip

The fabrication of the MEMS chip was divided into two parts: the SOI and the glass wafer. The SOI wafer selected was <100> orientation and p-type/boron doping for both handle and device silicon. The critical factor was the resistivity of the device and handle silicon. Since we were using the device silicon and handle silicon as two electrodes, it was critical to have the required resistivity. Resistance of 1-20 Ω-cm was desired and wafers of that resistance were selected. For the SOI wafer, a device silicon thickness of 3 µm, buried oxide thickness of 2 µm, and handle silicon of 500 µm were selected. For the glass wafer, a 500 µm thickness was selected. The details of the fabrication are discussed in the sections below.

3.3.1 Silicon on Insulator (SOI) Wafer

Prior to fabrication, the thickness of the silicon and silicon dioxide films must be determined. Using Filmetrics[8], the measurement of our purchased wafer's device silicon thickness ranged from 2.24 to 2.99 µm, with the maximum thickness at the center and the lower thickness towards the edges of the wafer. The thickness of underlying silicon dioxide did not vary a lot irrespective of the location on the wafer, the oxide measured 2.04 µm +/- 5 nm. The fabrication of the SOI wafer is divided into two lithography steps, *structure* and *structure metal*.

3.3.1.1 Structure

The first lithography step was to pattern the *structure* mask. The following are the steps that were used to pattern:

a. Spin hexa-dimethyl di-siloxane (HMDS): We used a Delta[9] spinner to spin HMDS at 3000 rpm for 40 sec and waited for a minute.
b. Spin S1827: Using a dropper we poured three to four drops of S1827 onto the Delta™ spinner, and then spun it at 3000 rpm for 40 sec.
c. Soft bake: Initial pre-exposure bake was done at 110°C for 60 sec.
d. Exposure: Using a Karl Suss EVG aligner in the hard contact mode, the wafer was centered under the mask and then exposed for 9 sec using the "I" line exposure.
e. Development: S1827 is a positive photoresist, so the photo active compound in the exposed region changes phases and was removed by using a base developer (MF 319) for 40 sec with slight manual agitation. We intermittently checked the resist for

[8] Filmetrics F20, San Diego, CA
[9] Karl Suss, Garching, Germany

complete development by inspecting it under a stereo zoom microscope. Figure 3-8 illustrates the test area on the wafer after complete development of resist.

f. Hard bake: The resist was then hard baked on hot plate at 110°C for 90 sec to drive away any remaining solvents in the resist and to improve the adhesion of the resist to the wafer surface and toughen the resist as RIE etch mask.

g. Descum: The final step in our photolithography was to clean up any undeveloped resist using a low power asher (isotropic dry etching). The recipe used for ashing is "Descum_300_0_0_400_3," where we use 300 sccm of O_2, at 400 W power for 3 minutes.

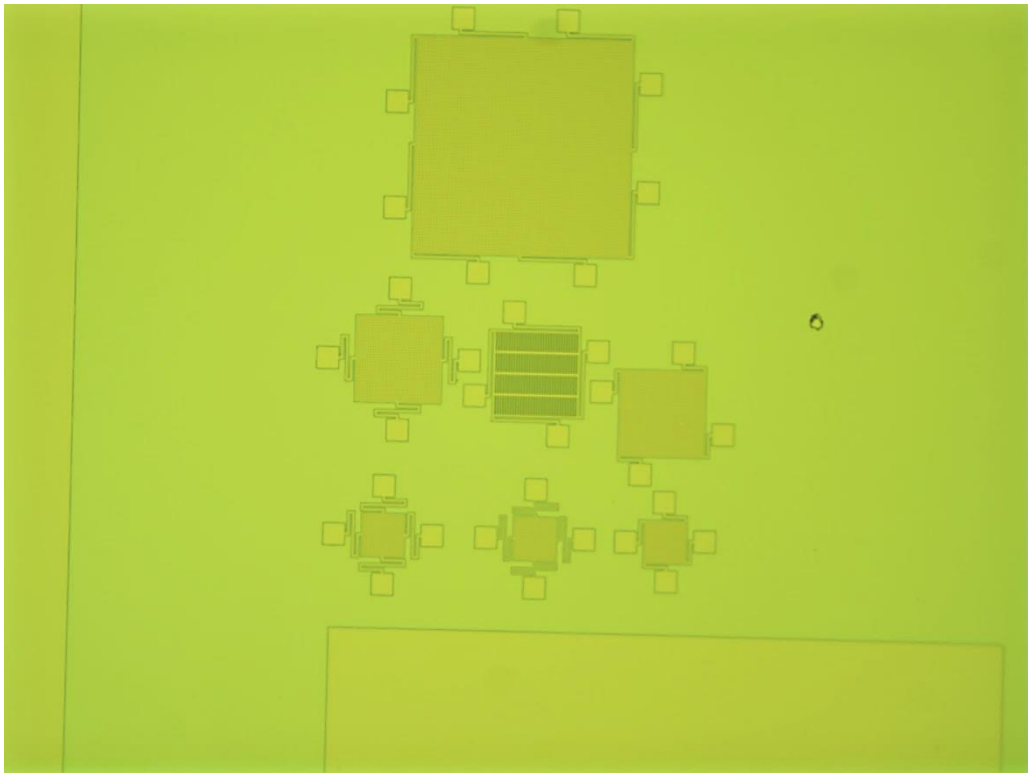

Figure 3-8: Microscope optical image after lithography and development of the resist and patterning *structure* mask

Once the above lithography steps were completed, the final resist thickness was measured using a Tencor[10] step profilometer. After measuring it at three different areas the average step height was 2.621 µm.

The first bulk micromachining step was to etch the structure silicon using the Unaxis[11] deep reactive ion etcher (DRIE). Using DRIE, high aspect ratio anisotropic silicon structures can be etched. In our design the structure silicon is approximately 3 µm. We used a Bosch recipe detailed in Table 3-1, which illustrates the three different stages of DRIE. First the surface was passivated, and then it was cleaned and etched so that the etching was only vertical and the sidewalls were passivated from the passivation cycle.

Table 3-1: DRIE Bosch process details

DRIE process	Time in seconds	RF power in watts		Gasses in sccm				Pressure in mTorr
		RF1	RF2	C_4F_8	SF_6	Ar	He	
Passivation	5	1.0	825	70	0.5	40	5.18	23
Clean	2	9.0	825	0.5	50	40	5.18	23
Etch	6	9.0	825	0.5	100	40	5.18	23

As DRIE etching is a function of the area of the silicon that has been etched, we typically see etching of 0.6 µm/cycle for the process described in Table 3-1. Also, since there is a ~30 nm-layer of native oxide, it takes certain cycles to ensure that the native silicon oxide is etched before the etching of silicon starts. We first used the "Bosch 7" recipe that has seven DRIE cycles to etch silicon. To confirm that all the exposed silicon had been etched, we used

[10] KLA Tencor, Milpitas, CA
[11] Plasma Therm, St. Petersburg, FL

Filmetrics as an end point detector. After our initial inspection, we found silicon in some areas and confirmed that we did not see any trace of the silicon dioxide. We then etched for another 7-DRIE cycle, anticipating that some initial cycles will be needed to etch the native oxide and to achieve a ~ 20% over-etching of silicon. Once post DRIE etching and inspection using Filmeterics, we found no silicon, and we could visualize the oxide film, since it contrasted with the gray color of silicon. The oxide was accurately measured using Filmetrics.

Once we confirmed that the structure silicon was etched, the next step was to etch the oxide using a Unaxis reactive ion etcher (RIE). The RIE tool used had an electrically conductive chuck where the wafer was placed. We used gasses like CHF_3 and O_2 at low pressure and applied a strong RF field created by chemically reactive plasma, the high energy ions from which were used to etch materials on the wafer. The etching of silicon was done using "S_etch" recipe and the parameters of the recipe are detailed in Table 3-2.

Table 3-2: RIE process parameters

RF power in watts	Gasses in sccm		Pressure in mTorr
	CHF_3	O_2	
200	45	5	40

We typically observed a etch rate of silicon dioxide that varied from 25-30 nm/min for this recipe. To etch the 2000 nm (or 2 µm) oxide, we first etched for 65 min and observed that the silicon oxide was not etched completely, so we etched for additional 25 min to ensure that all the silicon oxide was etched with a 10-20% over-etch. Finally, after additional etching, we inspected using the microscope and Filmetrics to see if there was any remaining un-etched oxide. Our inspection found there was no oxide left. Figure 3-9 is an optical image illustrating the

bonding area, fuse area, busbar, and MEMS plates and springs after the RIE etch process. A magnified image illustrating the 2x2 array area is shown in Figure 3-10, and a more magnified view of the springs and release holes is shown in Figure 3-11.

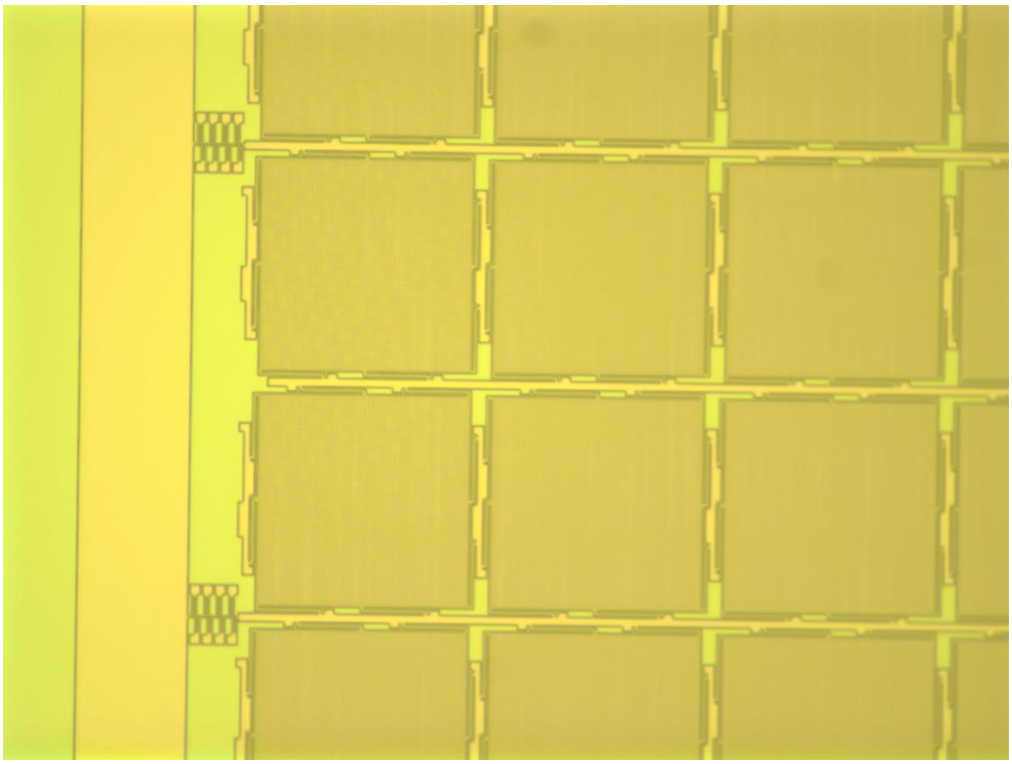

Figure 3-9: Microscope image after DRIE and RIE

Though the process used above for DRIE and RIE was selective and etched photo resist slowly, having at least 1:1 ratio of the material to be etched and the photoresist is a good fabrication technique. Once the silicon dioxide was etched, we inspected the wafers and saw that there was still photoresist left. To remove the remaining photoresist we soaked the wafer first in acetone, followed by methanol, and then DI water. This process removed most of the photoresist and the leftover scum was removed by the descum process, which consisted of isotropic etching of photoresist in an oxygen rich environment. The recipe "300_0_0_400_10" was used to etch all the photoresist and the wafer was etched for 10 minutes.

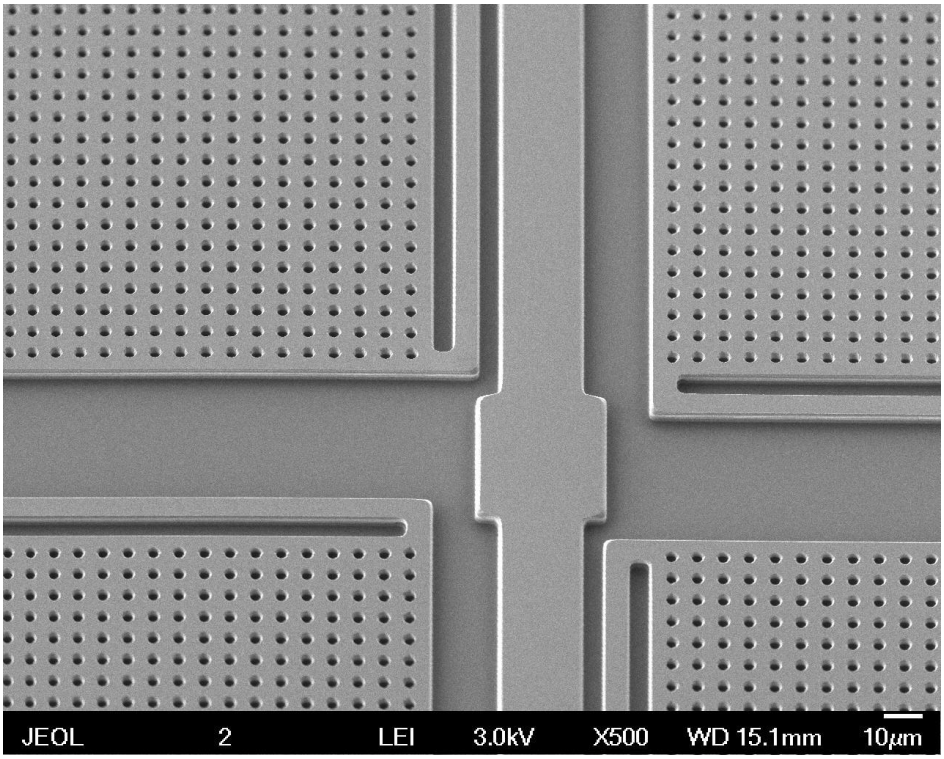

Figure 3-10: Scanning electron microscope (SEM) image illustrating a 2x2 array area

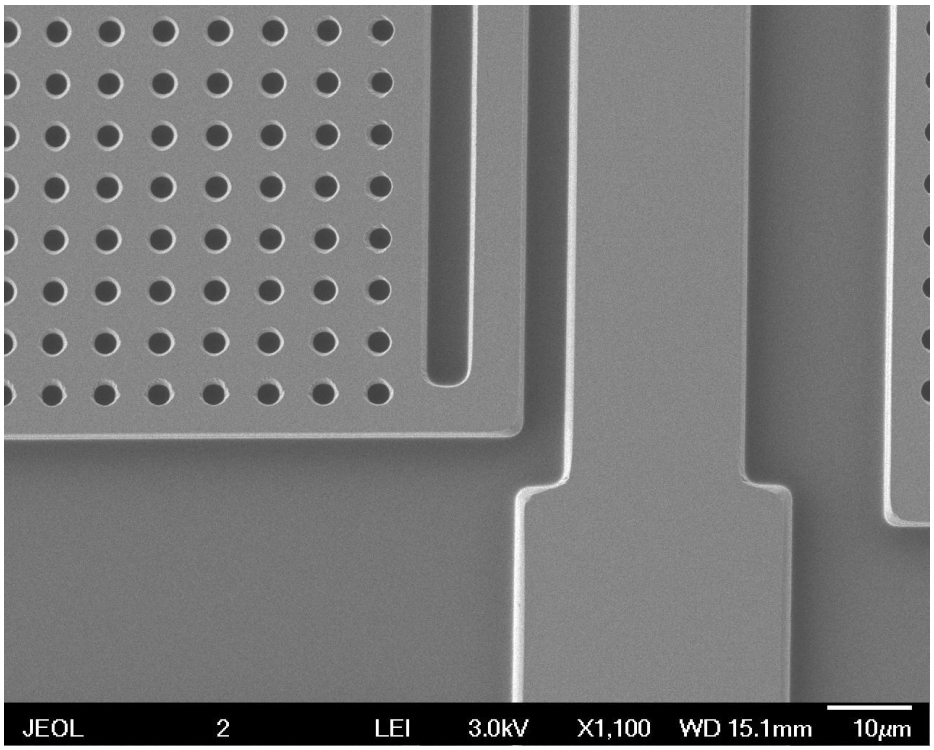

Figure 3-11: Zoomed-in SEM image illustrating the busbar connecting the mirrors and release hole and spring area

The above steps complete processing of the first mask, *structure*, an important mask step that defines the etch area for the handle silicon that defines the MEMS plate, spring, busbar, and chip outline. The next mask, *structure metal*, defines the area where we need to metalize the silicon to define the bond pad and chip bonding areas.

3.3.1.2 Structure Metal

To process the *structure metal* mask, we first deposit 30 nm of chromium as an adhesion layer and then 300 nm of gold in a sputter tool. The first choice of material for the adhesion layer was titanium, but the 49% hydro fluoric acid (HF) we use during the release step attacks titanium, so we decide to use chromium as a seed layer. Using chromium creates chances for chromium oxide to form on the target, which leads to initial sputtering. To avoid that risk, the chromium was pre-sputtered for 5 minutes without opening the shutter between the target and the wafer. The metals were sputtered using a RF magnetron sputter tool at 29 sccm of argon gas, with 360 W RF power and 2 mTorr pressure.

The next steps were patterning the metal with the *structure metal* mask and etching it. First HMDS was spun at 3000 rpm for 40 sec, next the S1813 photoresist was spun at 3000 rpm for 40 sec, and then the resist was baked at 110°C for 60 sec. The resist was then exposed using an I-line aligner for 15sec, an exposure/dose twice the typical exposure time used for S1813. We wanted to expose the resist longer so that the resist in the release hole areas was also exposed and developed completely; if left undeveloped the resist will mask and impede the etching in that area. The minimum feature size on the *structure metal* mask was 30 µm and over exposure and overdevelopment will cause the features to be smaller (~ 20 µm), however, that will not cause any problems as the release features are at 3 µm pitch and even when we release the structure we will have oxide under the anchor and busbar area. The typical resist development time was 60

sec, the resist was overdeveloped for an additional 20 sec (total 80 sec) to ensure that all the resist in the release hole areas was developed. The resist was then hard baked at 110°C for 90 sec, and then any undeveloped resist was removed in the descum step using recipe "300_0_0_400_3" for 3 minutes. The wafer was then inspected using a differential interface contrast setting on the microscope to ensure that all the resist was developed from the release hole area. Gold (Au) was then etched using TFA gold etchant, a potassium iodine-based gold etchant from Transene[12] with an etch rate of 2.8 nm/sec. During etching, we saw that the Au in the larger areas cleared in 2 min 20 sec, and then we over-etched for an additional 40 sec to ensure that all the Au had been etched.

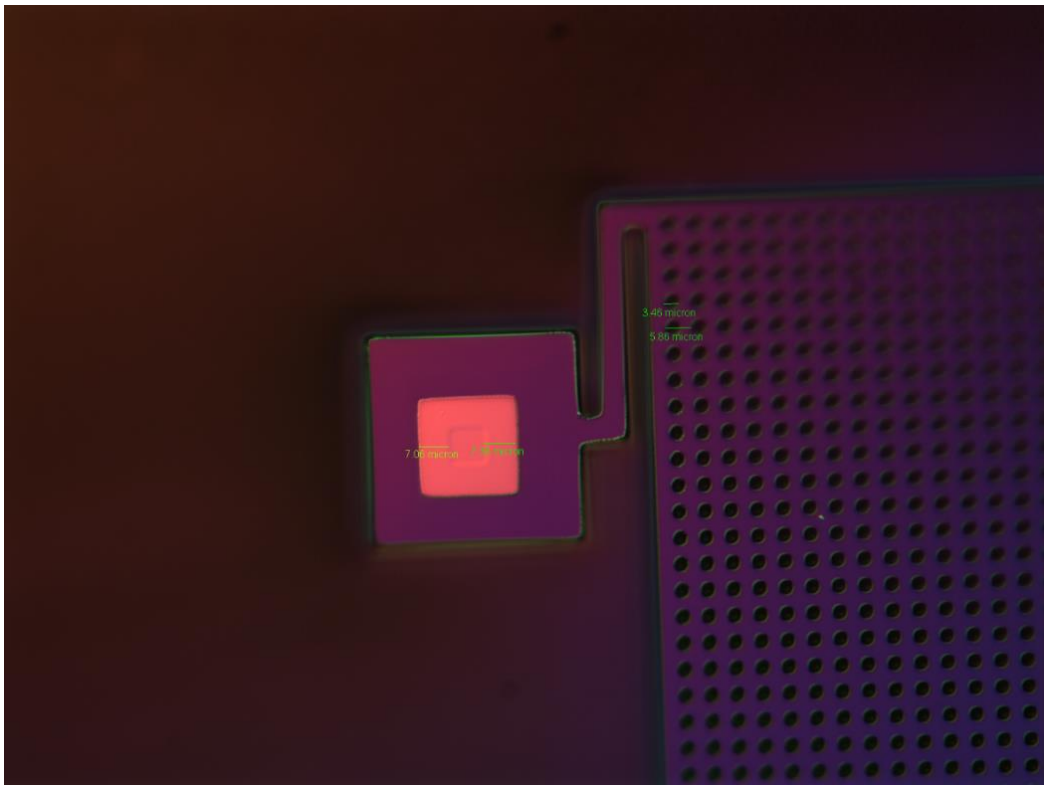

Figure 3-12: Undercut in chrome films after etching for 75 sec, with undercut of 7 µm

[12] Transene Co Inc, Danvers, MA

Next, Cr was etched using Transene Nichrome, a ceric ammonium nitrate-based etchant with an etch rate of 5 nm/sec. One distinct characteristic we observed about the Cr etchant was that for the initial few seconds it seems that no etching was going on, and then, suddenly after 20 sec, we can see that the Cr etching has started. We feel that this occurs because the etchant was slowly etching the chromium oxide first and then, once done, starts etching the chrome. We etched for about 75 sec, which was 40 sec more than the calculated time. With chrome etching, it was difficult to spot the end point visually because the color chrome film and silicon are very similar, so an additional overetch was not harmful to the design and ensures that all the chrome was etched from the release hole areas. Since we over etched the Cr, we found the undercut was close to 7 µm as shown in Figure 3-12. Following this, the wafer was then inspected and looked like the images shown in Figure 3-13 and Figure 3-14. The undercut of 7 µm was excessive, but still sufficient chrome area to adhere the gold and provide good bond area. In the subsequent wafers fabricated, the undercut was approximately 2 µm, which was what we expected.

The wafer was then inspected to ensure that the structure, metal, and all the springs look good, a protective resist was spun and hard baked, and then the wafer was diced into 8 x 10 mm^2 chip size using K&S dicing[13]. The diced chips were then cleaned using an acetone soak and slight spray for 5 minutes followed by methanol soak for 3 minutes and then an isopropyl alcohol (IPA) soak for 3 minutes.

[13] K & S Dicing, San Jose, CA

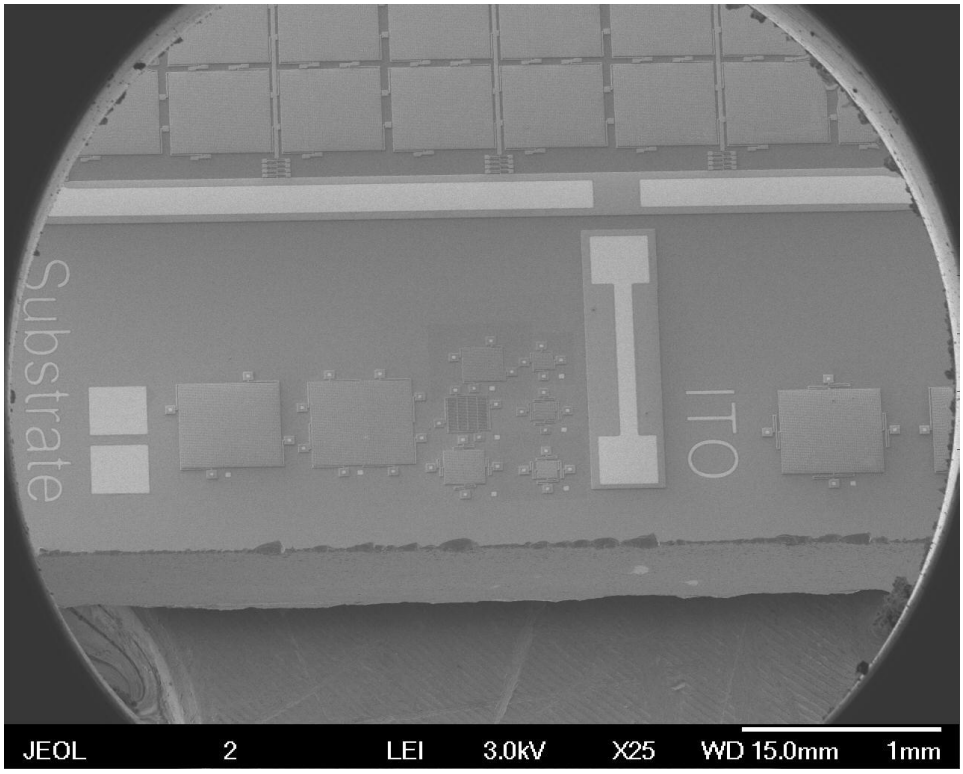

Figure 3-13: SEM image of test area and initial array of the structures

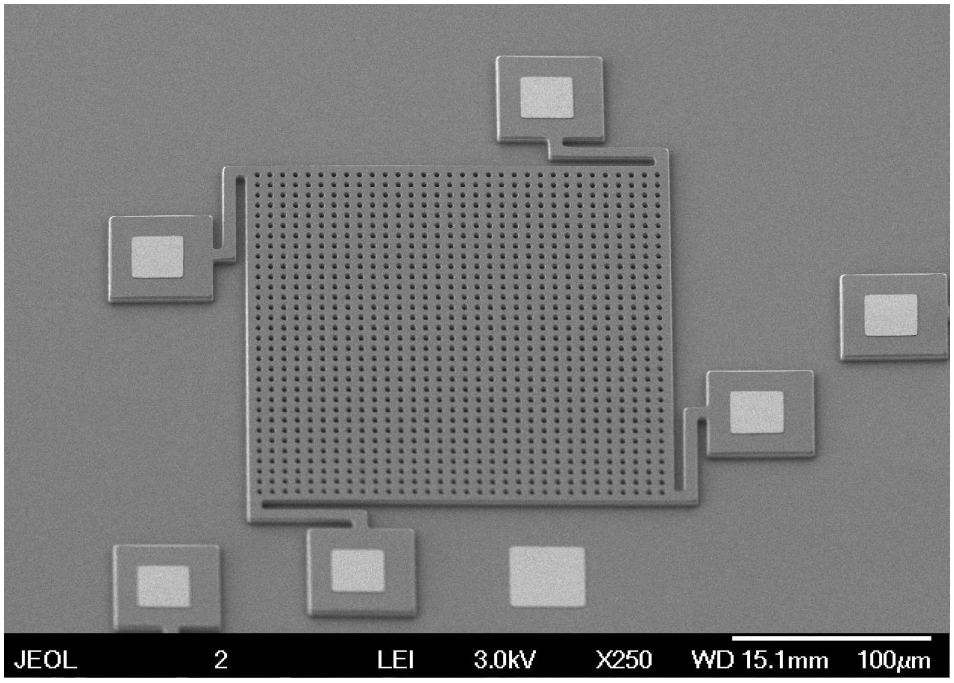

Figure 3-14: SEM image of a 200 x 200 µm plate after *structure* and *structure metal* mask

3.3.2 Release of SOI Chips

Finally, using clean DI water, the chip was rinsed and made ready for the release step. In the release step, 49% HF was used to etch the buried oxide and release the structure. The release holes are circular with 3 µm diameter and 9 µm spacing, so to ensure the oxide was etched completely, we needed to etch 3√2 µm, 4.24 µm. The etch rate of thermally grown silicon dioxide is 2.8-3.3 µm/min in 49% HF [55] (the variation comes from the way the silicon dioxide is grown). Assuming a 3 µm/min etch rate, we feel that etching it for 75 sec will remove 3.75 µm of oxide, which will leave little oxide area in the middle of four release holes.

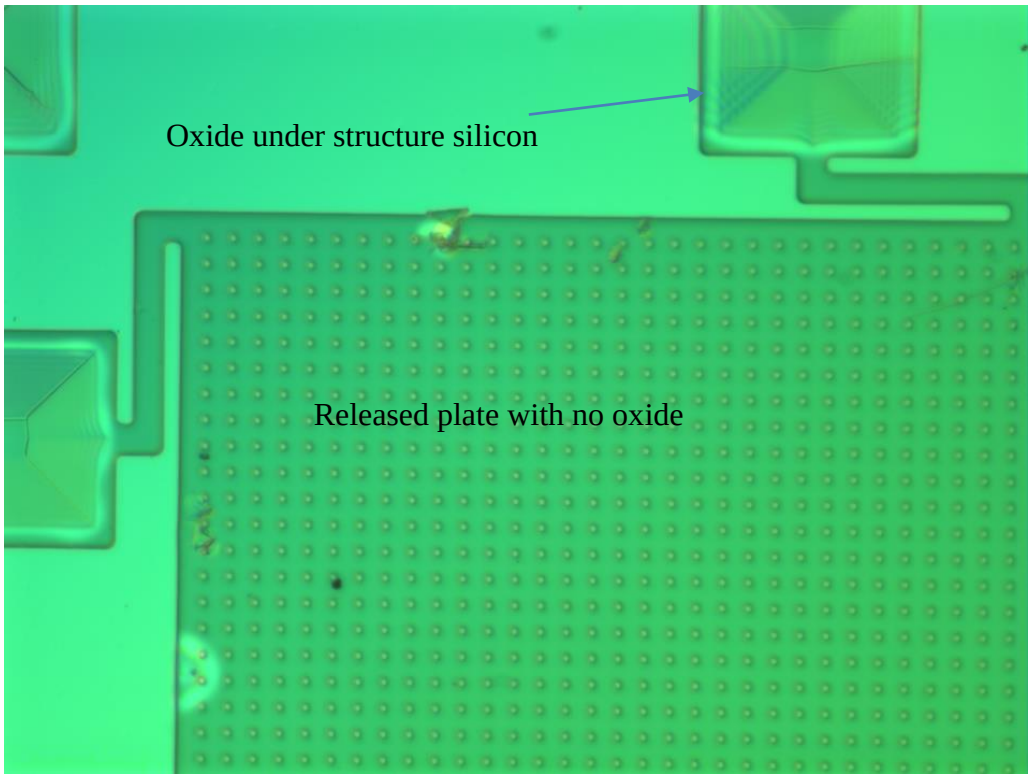

Figure 3-15: Microscope image illustrating oxide in bond pad area and no oxide under the MEMS plate area after 75 second of release in 49% hydro fluoric acid

After etching, the chip was rinsed in gentle running water and then carefully transferred to clean IPA. The chip was soaked in IPA for about 5 minutes and then transferred into another clean IPA solution to replace all the water with IPA. The chip was then transferred to a plate and

kept in an oven at 90°C for 15 minutes so that all the IPA evaporated. If we had found that the MEMS plate was sticking in the release process, we would have used the critical point dryer, but it was unnecessary. Figure 3-16 is a dark field microscope image that shows the un-etched silicon oxide as the dark area in the busbar. The next step was to fabricate the glass chip and then finally bond the glass chip and the SOI chip together to make the MEMS chip.

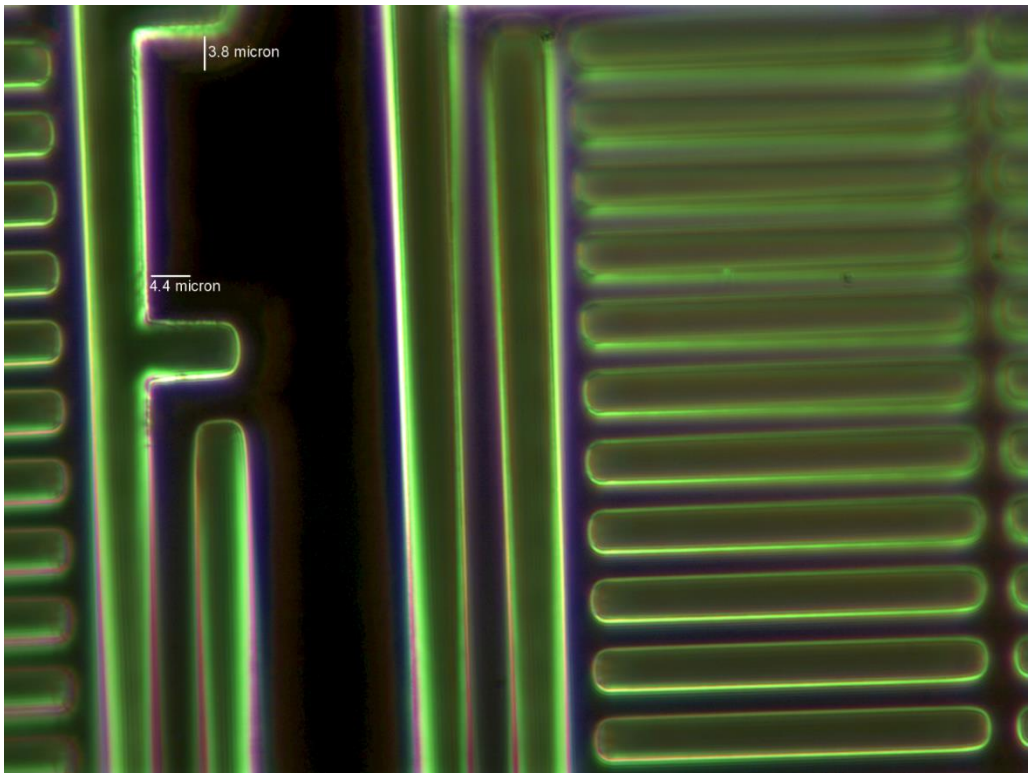

Figure 3-16: Undercut of silicon oxide (~4 µm)

3.3.3 Glass Wafer

We start with a 4-inch borosilicate glass wafer, with a 500 µm thickness, double-side polished, and a surface roughness less than 1.5 nm. The first step in fabrication was the indent mask, as to bond the SOI chip to the glass lid, at least 250 nm of Au was required on both SOI and glass chip. We measured that the step height of the deposited Cr/Au on the SOI wafer was 300 nm, and we aim to deposit a similar thickness of metal onto the glass wafer. Since the SOI wafer is fabricated using surface micromachining, the metal on the bond pad area was above the

MEMS structure. To ensure that there was 200 nm gap between the glass lid and the MEMS structure, it is important to maintain the flatness of the glass lid. This meant we did not want to etch the ITO electrode area, and, to ensure that there is a 200 nm gap between the ITO electrode and the MEMS structure, we would need to indent the glass wafer, with the thickness of the indentation dictated by the gap between the ITO electrode and the MEMS structure.

Let us designate the indentation of the bond area as I_{glass}, the Au thickness on the on SOI wafer as Au_{SOI} and on the glass wafer as $Au_{glass,}$ and the gap between SOI and ITO electrode as $G_{glass\text{-}SOI}$. We have ITO on the electrode area and it will not be harmful to have ITO in the bond area, too, as long as the ITO in the bond and electrode areas were not connected. Having ITO in the bond area will also mean that we have to indent the glass less. Equations (3.1) (3.2) and (3.3) show that the indentation of the glass lid in the bond area should be less than 400 nm to ensure that there was a gap of less than 200 nm between the MEMS structure and ITO electrode. The fabrication of the glass wafer was divided into three sections: first was the indent, second was the ITO patterning, and the third was the ITO metal or bond pad metal.

$$Au_{SOI} = Au_{glass} \sim 300\ nm \tag{3.1}$$

$$G_{glass-SOI} \leq 200\ nm \tag{3.2}$$

$$I_{glass} = Au_{SOI} + Au_{glass} - G_{glass-SOI} \tag{3.3}$$

3.3.3.1 Indent

The first step was to create an indent in the bond area of the glass wafer. To do that, we used photoresist S1813 as a masking layer and buffered oxide etchant to etch the glass in a controlled manner. Starting with a bare glass wafer, we pattern S1813 by doing the following:

a. Spin S1813 at 3000 rpm for 40 sec.

b. Soft bake S1813 at 110°C for 90 sec.

c. Expose the resist for 8 sec with *Indent* mask.

d. Develop the resist for 35 sec to ensure that all the resist is removed and then inspect it under the microscope.

e. Use the Tepla isotropic etcher to descum for 3 minutes.

We preferred to etch the glass wafer in BOE as oppose to HF or RIE, so that we could maintain the mirror-like glass surface after etching and etch using a less aggressive etchant to better control the depth of etching. The step height measurement with the resist was 1.9 µm, and BOE etches glass at about 25-30 nm/min [5, 37, 46, 55]. From that rate, we calculated that it should take between13 min 20 sec and 16 min to etch 400 nm of glass. We etched the glass for 14 min and, after inspection, did a step profile and found that the etch depth of glass was a near ideal 390 nm. This etch depth is good enough for what we wanted to achieve.

3.3.3.2 Indium Tin Oxide (ITO)

ITO was selected as the conductive material to be deposited on the glass wafer. The advantage of ITO was that it was electrically conductive and optically transparent for a wide range of wavelengths. The properties of the ITO film can be altered by varying the different deposition parameters, such as chamber pressure, gas flow ratio of argon and oxygen, and the temperature of the substrate.

A thin layer of ITO was deposited on glass wafer using a house-developed single RF magnetron sputter tool. A sputter target with a mixture of 95% indium and 5% tin was selected and the sputtering was performed using high-purity Ar and O_2 gas. [51, 52], the deposition parameters were selected to yield optically transmitting films, and the electrical conductivity of the films was then measured by varying the pressure, substrate temperature, and gas ratio. A 4-

probe station was used to measure the resistivity of the film, and the optical transmittance was measured using an optical spectrometer.

The deposition of the ITO film was done at 70 W for 20 min for all the above conditions. As Table 3-3 shows, the Ar/O_2 gas ratio of 20/20 at 1.15 mT pressure with a chuck temperature of 310°C yielded a 277.5 nm-thick film with a resistivity of 66.81 ohms-cm. The film showed optical transparency of over 90% for a 632.8 nm-laser.

Table 3-3: ITO film conductivity with various processing parameters

Ar/O_2 (sccm)	Pressure (mT)	Deposition Temperature (°C)	Thickness (nm)	Conductivity (1/ohm-cm)
20/10	2	250	2770	6.94E-06
20/10	2	280	2206	1.02E-06
20/10	2	310	3060	9.49E-07
20/10	1.5	250	2514	1.86E-06
20/10	1.5	280	3122	1.31E-06
20/10	1.5	310	3133	1.16E-06
20/10	1.15	250	3094	1.58E-06
20/10	1.15	280	3082	1.38E-06
20/10	1.15	310	3078	1.30E-06
10/20	2	250	164.0	7.47E-01
10/20	2	280	87.62	6.29E-01
10/20	2	310	104.3	6.61
10/20	1.5	250	100.4	2.54
10/20	1.5	280	110.6	4.8
10/20	1.5	310	125.6	28.5
10/20	1.15	250	86.6	5.2
10/20	1.15	280	50	9.08
10/20	1.15	310	57	11.06
20/20	2	250	249.1	15.27
20/20	2	280	215	25.4
20/20	2	310	194.2	30.7
20/20	1.5	250	258.7	12.61
20/20	1.5	280	241.6	26.86
20/20	1.5	310	248.5	36.7
20/20	1.15	250	258.6	20.07
20/20	1.15	280	286.8	40.49
20/20	1.15	310	277.5	66.81

Once the ITO film was deposited, we tried etching the film using both dry and wet etching techniques. Most of the wet etchants did not have any effect on the ITO films. We tried dry etching in both RIE and DRIE systems, and the ITO film showed no etching in CF_4, O_2 and SF_6 plasmas [50]. Finally, we decided to use the lift off process to pattern the ITO film. In preliminary experiments we wanted to anneal the film to 310°C; however, in the lift off process, we cannot bake the resist to that high a temperature, so we decided to anneal the film after the lift off process was completed. In the process, we spun NR9-1500 PY photoresist at 3000 rpm for 40 sec and then did a pre-exposure bake at 150°C for 60 sec. We followed this with an exposure using the g-line aligner for 15 sec using the *ITO* mask and then a post exposure bake at 100°C for 60 sec. The resist was then developed in MF319 developer for 20 sec, and the features were then inspected under microscope.

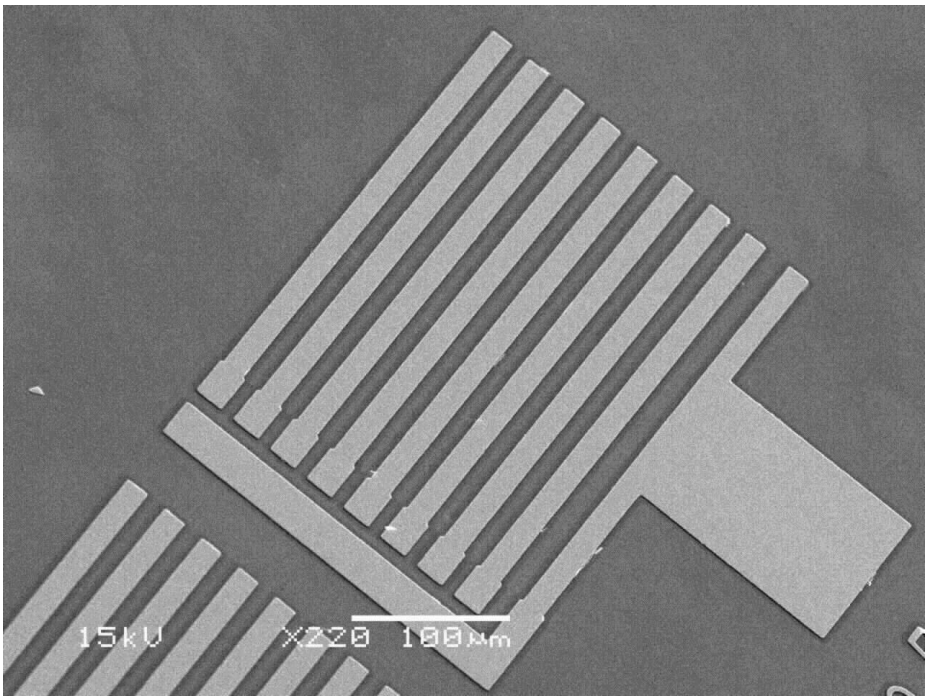

Figure 3-17: Post-annealing features of ITO after liftoff process

Once they looked good, ITO was deposited at a low temperature (~150°C). This required low-temperature deposition of ITO resulted in a highly resistive (Mohms) film. The resist was

then lifted off by soaking it in acetone/methanol. Once all the resist and the ITO above it was lifted off, the wafer was then annealed at high temperature (450^{o}C) in an oxygen environment, which reduced the resistance of the ITO film from Mohms to 40 ohms/square. Figure 3-17 illustrates a test feature that we used while developing the process for ITO film.

3.3.3.3 ITO Metal

The final lithography step in the glass wafer fabrication is patterning the *ITO metal*. Cr-Au was used as the ITO metal so that it could bond to the Cr-Au film on the SOI wafer through Au-Au thermal compression bonding. Cr-Au film was deposited using a sputter tool 2 mT pressure and 30 W RF source for 3 min (50 nm Cr) and 5 min (300 nm Au) respectively. After deposition, the metal was patterned using S1813 positive resist. S1813 was spun at 3000 rpm for 40 sec and then soft baked at 110°C 60 sec. It was then exposed for 8 sec and the resist was developed for 30 sec, followed by a hard bake at 120°C for 90 sec.

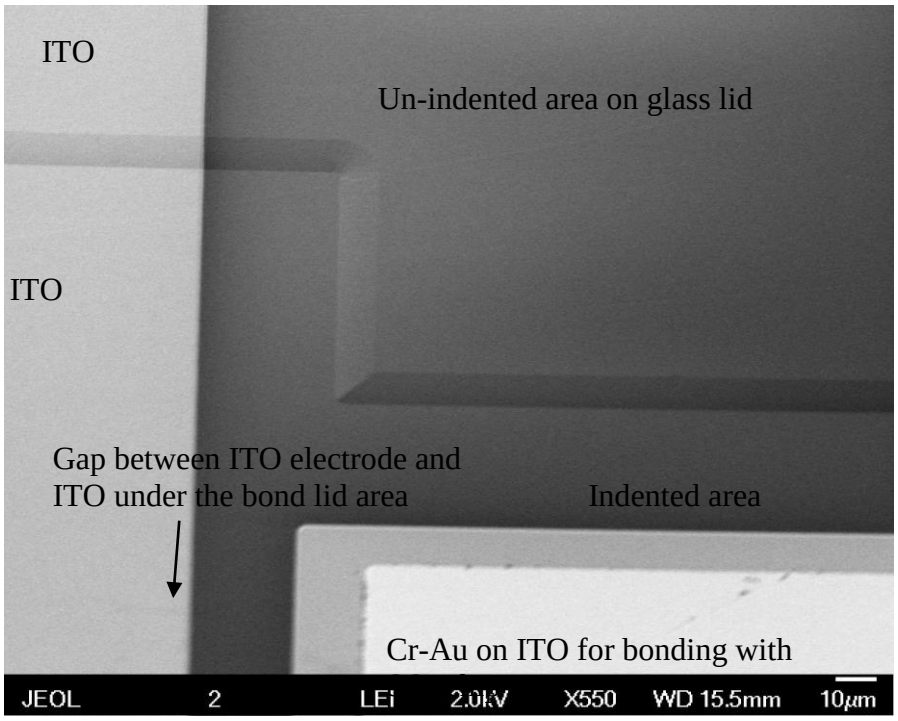

Figure 3-18: SEM image illustrating the indent area in the glass and the connection of the ITO electrode over the indent

Au was etched using a potassium iodine-based etchant for 3 min, followed by Cr etching using a cesium oxide based etchant patterned for 30 sec. It was easier to visualize chromium and gold etching point completion than it was on silicon. There was also a dicing line which was defined by the *ITO metal* mask. The *ITO metal* mask also defines metal on top of the ITO in the bond frame area as shown in Figure 3-18.

Once the etching was completed, a protective resist S1813 was spun, and the glass chips were diced into die size. The chips were cleaned using acetone, methanol and DI water and were then ready for bonding with the SOI chip. Now that the chip was fabricated, the next step was to perform electrostatic testing, optical profilometer inspection, and to bond the tested SOI chip to the glass lid. All these aspects are covered in the next chapter.

CHAPTER 4

PACKAGING OF THE MEMS CHIP AND TESTING OF THE COMMUNICATION SYSTEM

The previous chapter discussed design and fabrication of both the glass and SOI chips. The sacrificial oxide in the SOI chip was removed and the structure silicon was free to move in plane as voltage potential was applied across its electrode. This chapter discusses first the electrostatic actuation testing of the released SOI chip. This data is extremely important in the design of the transmitter unit as it gives us an estimate of what voltage will be required to actuate the MEMS structure. Once we are confident that the MEMS structure on SOI chip modulates, we can then bond the SOI chip to the glass lid and then the MEMS structure can even move out of plane when voltage applied across its electrode. This chapter next discusses the design and mounting of the bonded SOI and glass chip, also referred to as the MEMS chip. The last part of the chapter discusses the most critical part of the project, in which the commercial CCR is precisely bonded to the MEMS chip, and presents the benchtop testing of the bonded CCR.

4.1 Testing of MEMS Structures on SOI Chip

After the SOI chips were released, the structure plate can move towards the substrate (in-plane movement) once potential is applied between the two electrodes, presently in our system the gap between structure and substrate is 2 µm. Once we bond the glass lid to SOI chip, then we can even modulate the structure plate towards glass lid (out-of-plane movement), by applying potential between ITO and structure electrode, presently we aim to achieve a gap of approximately 200 nm between ITO and structure. The optical profilometer we use did not offer

the option of looking through the medium (glass), so we cannot test the out-of-plane movement of structure under an optical profilometer. We were able to test in plane movement of the structure and that gave us a good estimation of what actuation voltages were required for out-of-plane movement. We use an optical profilometer to take images of in-plane measurements and voltage was applied on the electrode by making contact to bond pads on the chip using fine-tip probes, which magnetically lock on to the stage and can be manually moved using a micrometer.

4.1.1 Testing Structures

The left side of Figure 4-1 is a snapshot of the mask layout of an SOI wafer (structure in grey, release hole in magenta, and structure metal in gold). Once the wafer was fabricated and released, this particular area was scanned using an optical profilometer. The test structures were a single representation of the MEMS plate along with various styles of spring and all the chips fabricated have these test structures. Testing this test structure area gives us an estimate about the pull in voltage behavior of all the designed MEMS plates and spring style. We added some high-resistance traces, also referred to as fuses that connect the voltage busbar to the electrode. This fuse element was designed to ensure that if there was a short in one of the elements in the chip, the entire chip was not compromised. The fuse acts as a high-impedance series resistor and is shown in Figure 4-2. Also there is an area for the glass lid chip to bond, called the bond frame area that connects the ITO electrode on the glass by bonding to the ITO electrode bonding area.

To test the in-plane movement of the structures we first take an image at zero potential, then using micrometer the probes were bought in contact with the bond pad. Once we ensure that the probes were making contact to the electrode, we apply voltage in steps and take an optical image for each voltage step. As we reach a particular voltage, the electrostatic force is higher

than the restoring spring force and the MEMS plate pulls into the substrate. That voltage is the pull-in voltage of that particular MEMS plate and spring configuration.

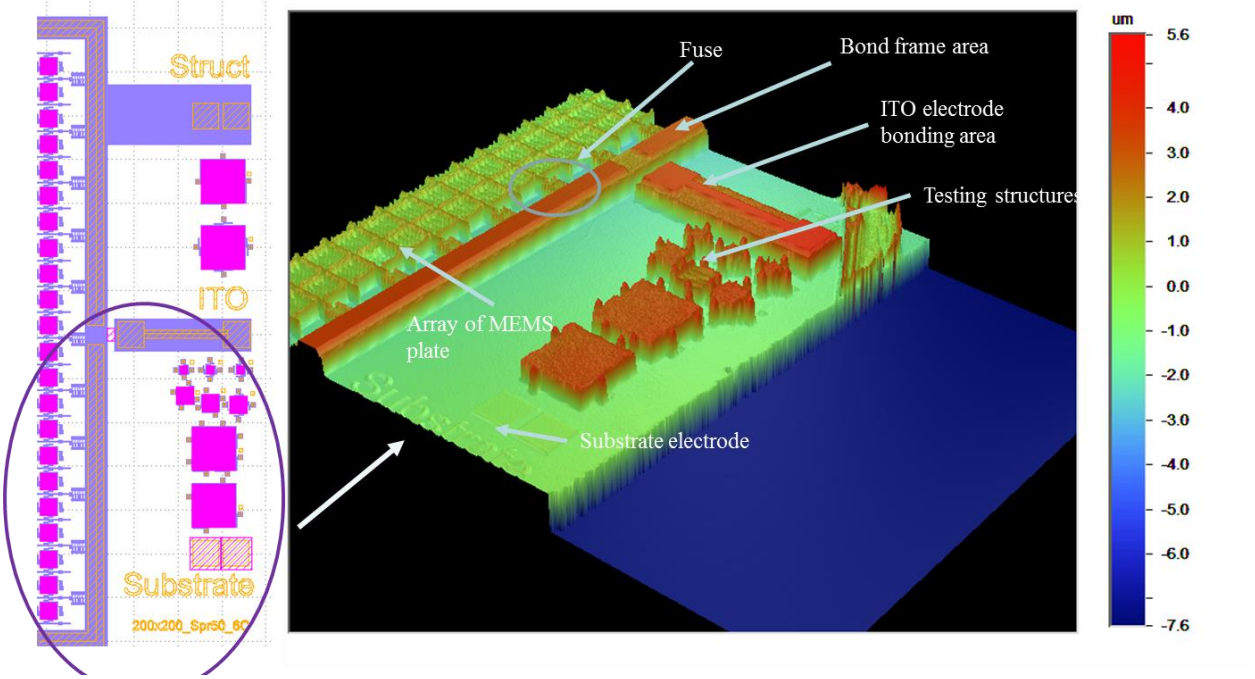

Figure 4-1: At left is the snapshot of the mask layout; at right is the optical profilometer image of the test area of a fabricated wafer.

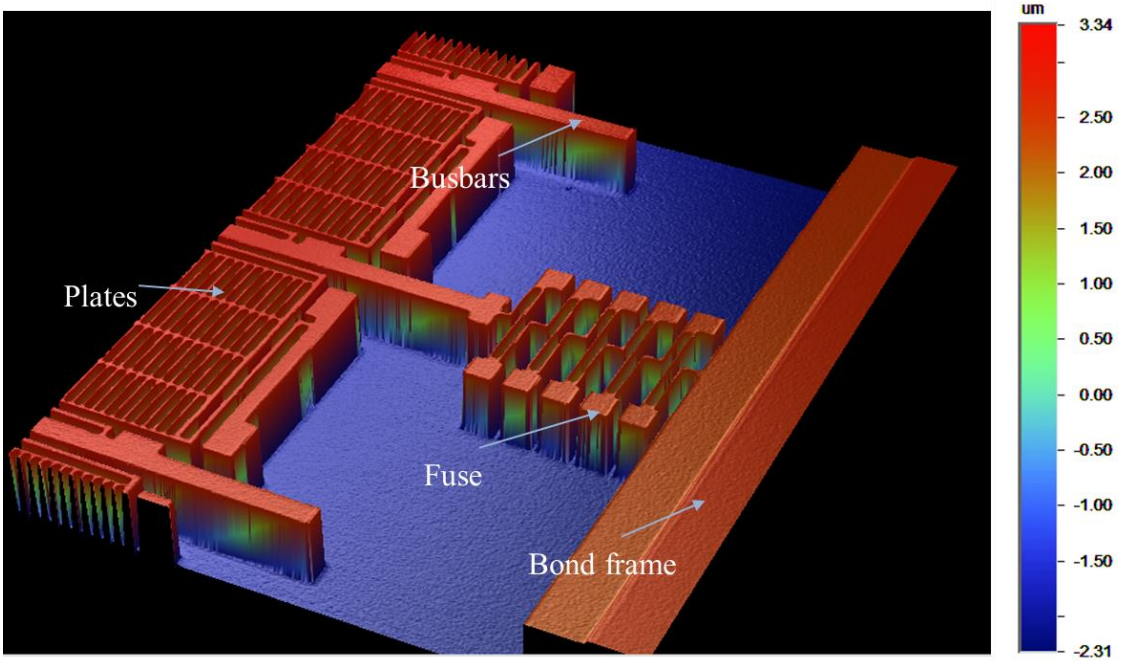

Figure 4-2: 3D optical profilometer image of fuse element in the circuit.

We started testing with the 100 µm plate configuration, it has two configurations one with serpentine (meander) and other with short spring. For 100 µm plate with serpentine spring, the measured pull in voltage was 9 V and for short spring 45 V. We also did a frequency analysis on serpentine spring structure and the measured resonance frequency around 200 Hz. As we knew from empirical calculations that as CCR modulation the pull in voltage for serpentine spring was low so we had an array of these styles. However the configuration of 100 µm plate with short spring, has high pull in voltage so we did not have an array of these structures, but had an individual element to test pull in voltage. Figure 4-3 and Figure 4-4 are optical profilometer images for serpentine and short spring styles respectively, on the left is the image at 0 V and on the right is the image once the plates pull in. The resonance frequency data mentioned above and going forward for different style of plates was measured using an optical profilometer with dynamic measurement capability (DMEMS). The resonance frequency data that we got from the DMEMS tool was in accordance with the calculated resonance frequency data from Table 2-2 and was presently good enough for testing the devices, a more accurate resonance frequency data can be obtained by using a vibrometer or similar tool.

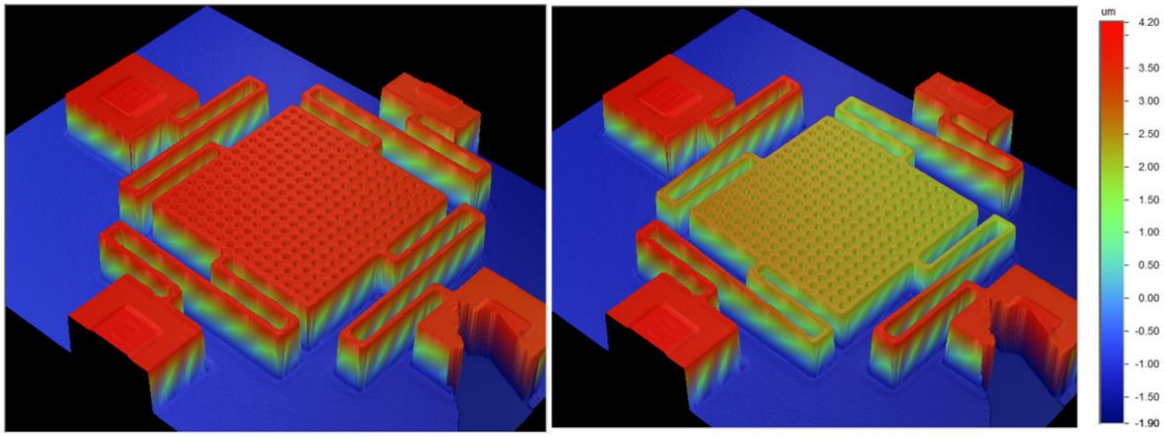

Figure 4-3: 100 x 100 µm MEMS plate with four serpentine springs showing the optical profilometer image at 0 V (left) and at 9 V (pulled in) (right).

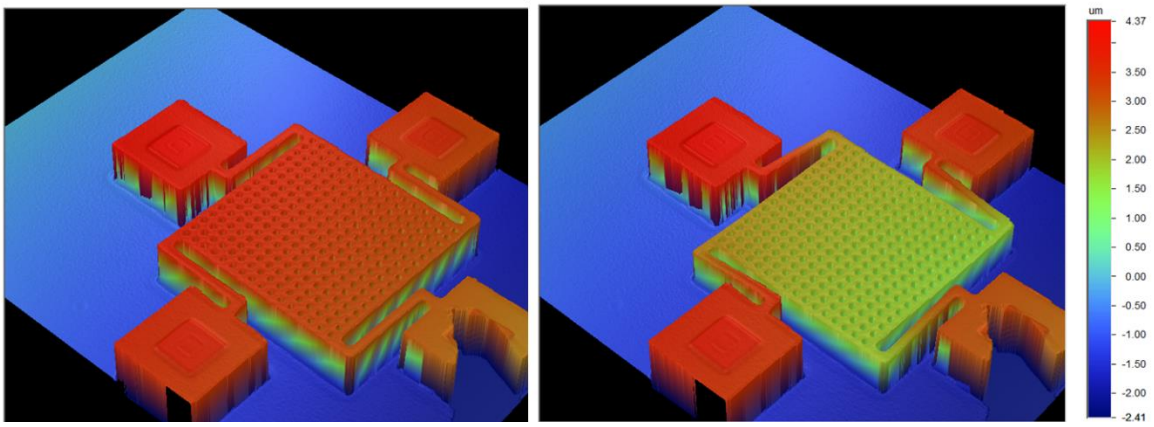

Figure 4-4: 100 x100 µm plate with short spring showing the optical profilometer image at 0 V (left) and at 45 V (pulled in) (right).

The 200 µm plates have three different spring configurations: meander (200 µm), long (150 µm), and short (50 µm). The serpentine spring configuration has the lowest pull-in voltage of 5.5 V, and the long spring style have pull in voltage of 7 V and short spring has a pull-in voltage of 20.8 V. For high-speed data transmission, the short spring topology works best as we performed a frequency analysis on this chip and found that it has a resonance frequency of 18 kHz, while that of the long spring style in 2 kHz range and serpentine spring was 50 Hz. Figure 4-5 shows an optical profilometer 2D analysis of a 200 µm plate at 0 V. The 2D scan appears to show that the release holes are not all the way through; however, that is an artifact of the resolution of the profilometer. Also, a step height of 4.2 µm includes the 2 µm sacrificial oxide, 2 µm of silicon, and 0.2 µm of metal. The thickness of the structure silicon seems smaller in this area, or perhaps the tool was not calibrated properly and that is the reason for the height disparity. Once we apply 4 V between the structure and the substrate, the MEMS plate pulls in by 1 µm as seen in Figure 4-6. One of the important things to note is that the MEMS plate is flat when it moves in and out of plane. Also noteworthy is that one side of the spring moves down and the other side of the spring moves up, very slightly (~ 100 nm) this movement of spring can be seen in plots in Figure 4-5 and Figure 4-6.

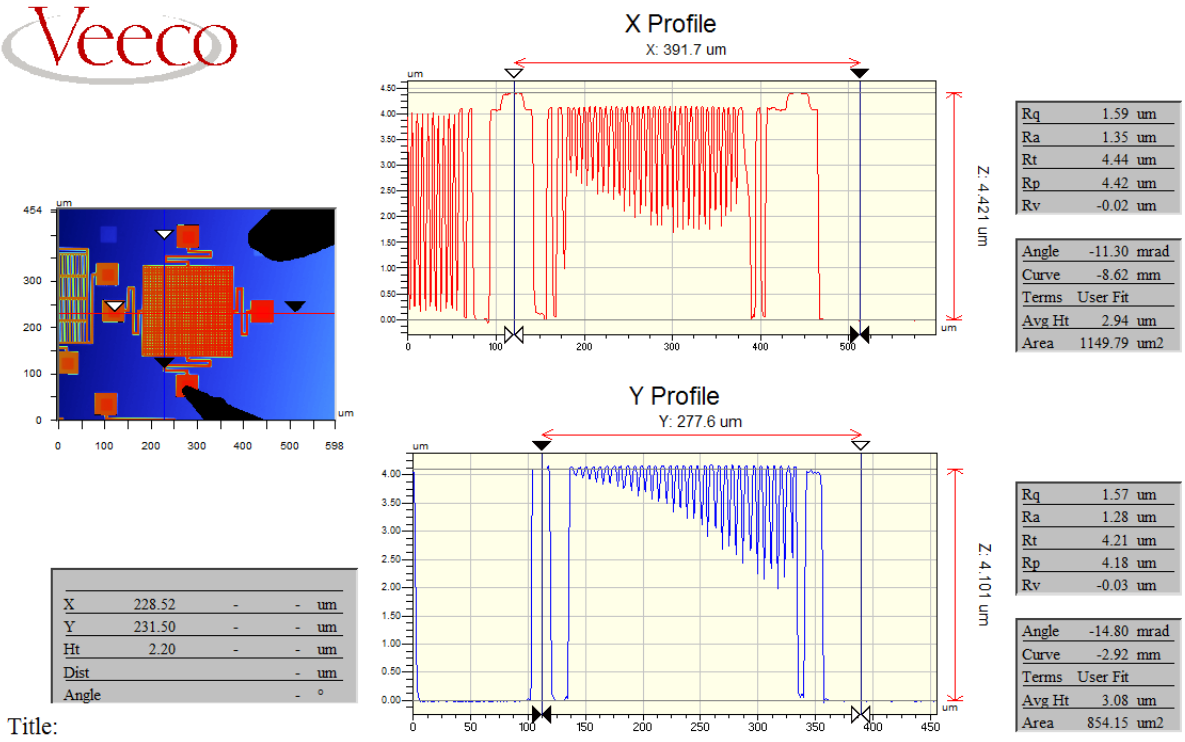

Figure 4-5: Optical profilometer 2D analysis of 200 x 200 µm plates at 0V

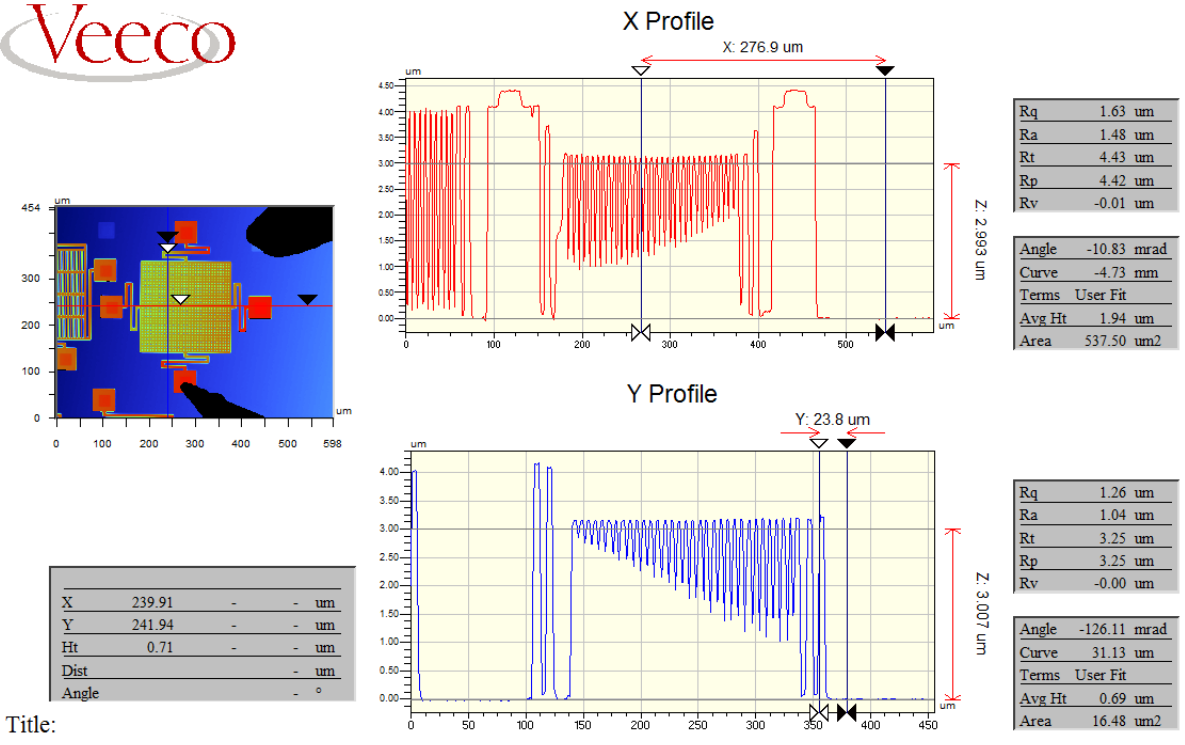

Figure 4-6: Optical profilometer 2D analysis of 200-µm plates at 4 V

The 500 x 500 µm plate has four different spring designs: serpentine (450 µm); long (150 µm); four short springs (50 µm); and eight short springs (50 µm). We knew that the serpentine and long spring designs will have the lowest pull-in voltage; however, their resonance frequency was below 100 Hz. The four- and eight-short-spring designs have low pull-in voltage and resonance frequency greater than 400 Hz. The pull in voltage for serpentine, long spring, four short spring and eight short springs measured 1.2 V, 1.4 V, 2.4 V and 3.7 V respectively. Figure 4-7 and Figure 4-8 show a 3D optical profilometer representations of the four-small-spring configuration at 0 V and pull-in voltage. The pull-in voltage information of all styles of plate and springs is tabulated in Table 4-1.

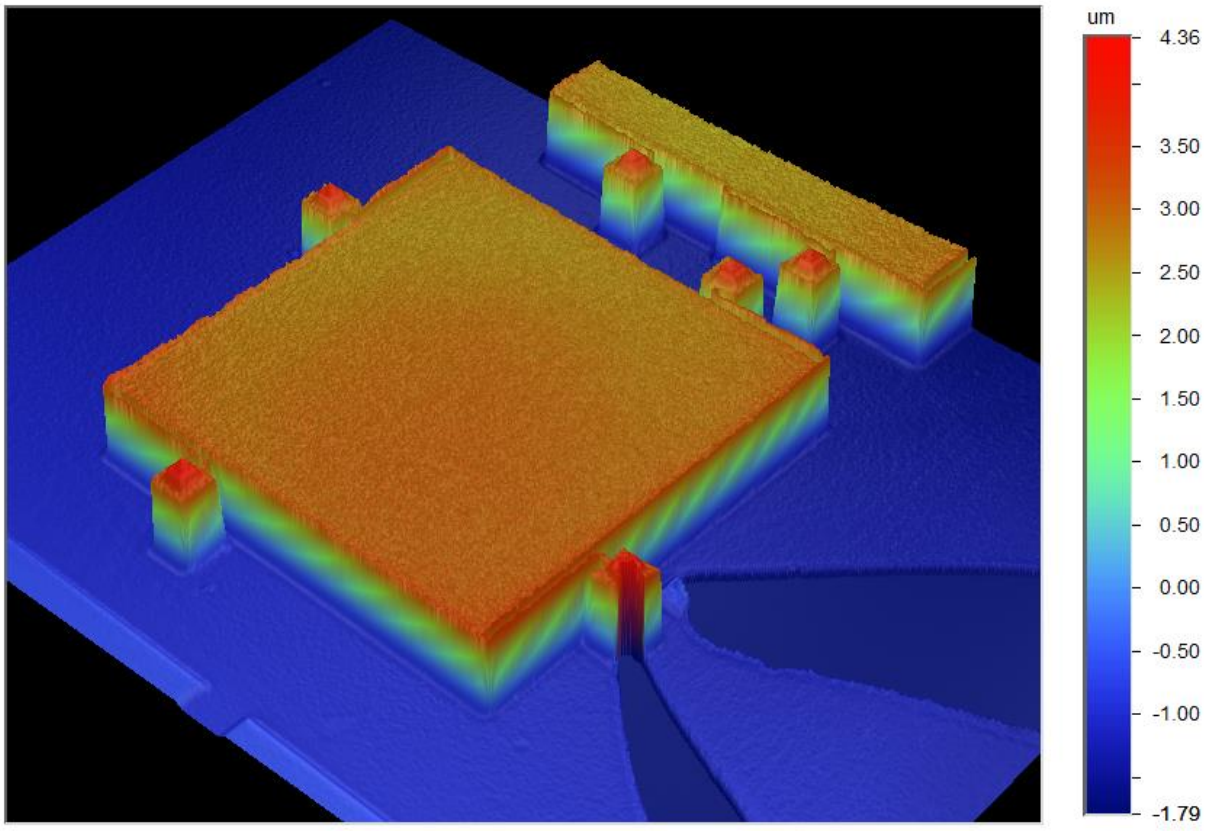

Figure 4-7: 3D analysis of 500 x 500 µm plate at 0 V

From Table 4-1, we see that the pull in voltage measured were much lower than the calculated values in chapter 2, the reason for that is the calculations made in chapter 2 were

almost a worst case scenario, considering simple spring Equations, if we perform a FEA analysis then we will find that the simulated pull in data is more in accordance to the measured data. We also noticed that the pull in voltage trend that the calculated values had in chapter 2, is similar to the pull in voltage measured in Table 4-1.

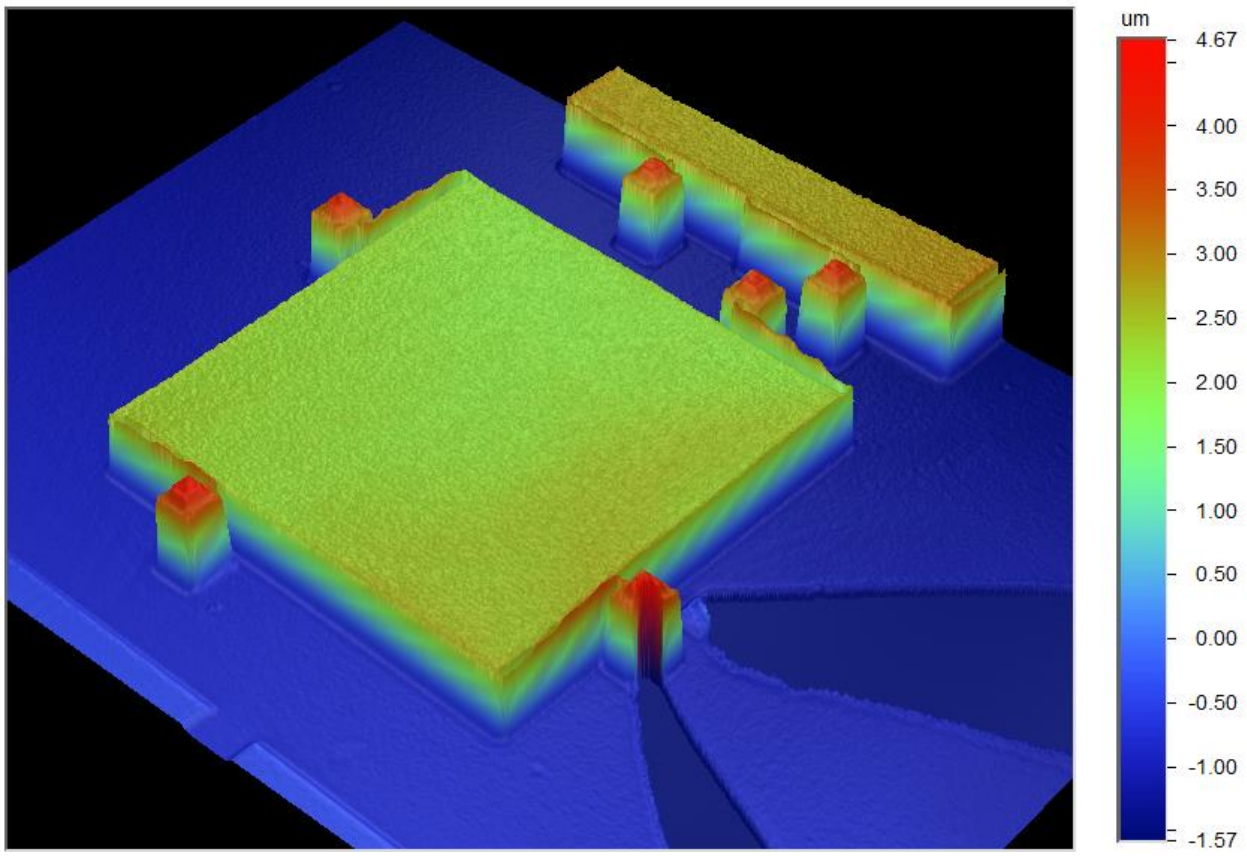

Figure 4-8: 3D analysis of 500 x 500 µm plate at 2.4 V

From the eight array design that is tabulated in Table 4-1, we feel that 100 µm plate with 200 µm long spring, 200 µm plate with 150 and 200 µm and 500 µm plate with four and eight 150 µm have battery operated pull in voltage and operate at greater than 400 Hz modulation frequency, so chips having array of above mentioned styles were selected for final transmitted unit application. The 200 µm design though can operate at high frequency (18 kHz), however has higher pull in voltage and similarly for 500 µm design with 450 and 250 µm long spring, have

low pull in voltage but operate at low frequency. So array of these designs were not selected for final transmitted unit application.

Table 4-1: Pull-in voltage measured for various MEMS plate and spring styles compared to calculated pull in voltage from Table 2-2

Plate size (in µm)	Spring length (in µm)	Number of springs	Calculated pull in voltage (in Volts)	Measured pull in voltage (in Volts)
100x100	200	4	10.14	9
200x200	55	4	35.18	20.8
200x200	150	4	7.81	7
200x200	200	4	5.07	5.5
500x500	450	4	0.6	1.2
500x500	250	4	1.45	1.4
500x500	150	4	3.12	2.4
500x500	150	8	4.42	3.7

4.1.2 Testing Array

Once we tested the individual MEMS plates next we started testing the array. At the lowest magnification level of the optical profilometer, we could only see one quarter of the arrays. So we tested quarter of an array each time, first we would take an optical profilometer image of the MEMS structure at zero potential. As seen from Figure 4-9, the MEMS structure at 0 V was completely flat.

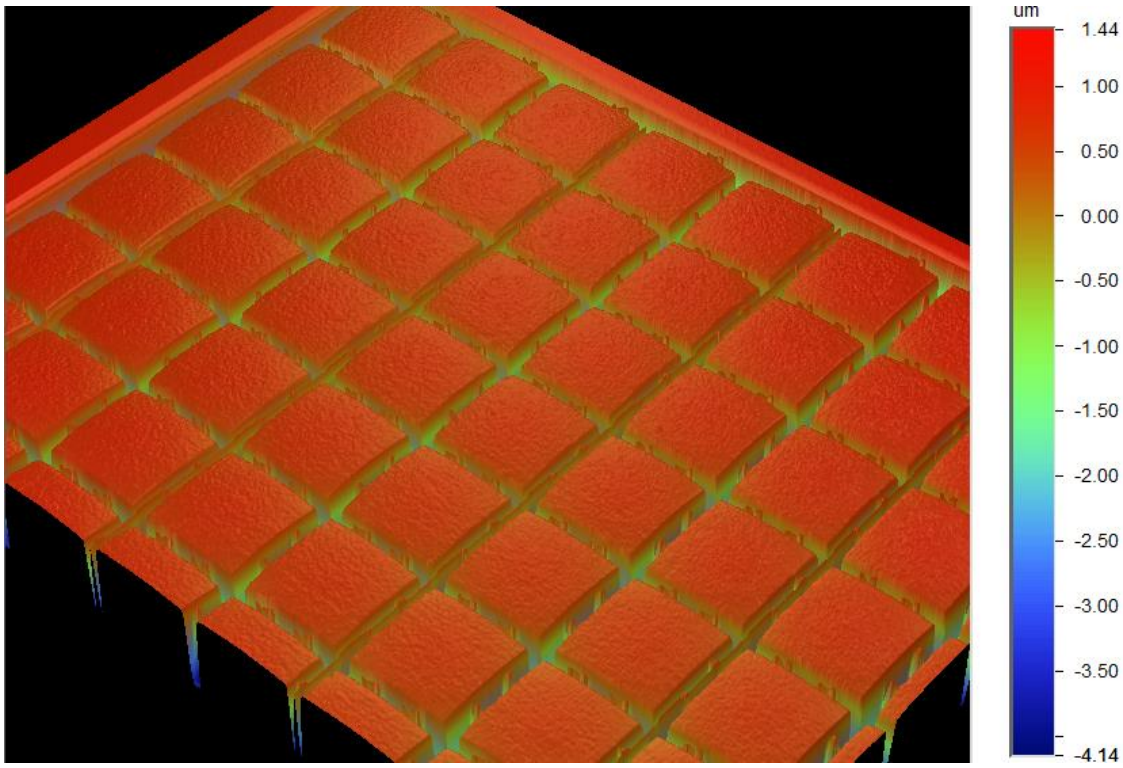

Figure 4-9: One-quarter of the MEMS array at 0 V

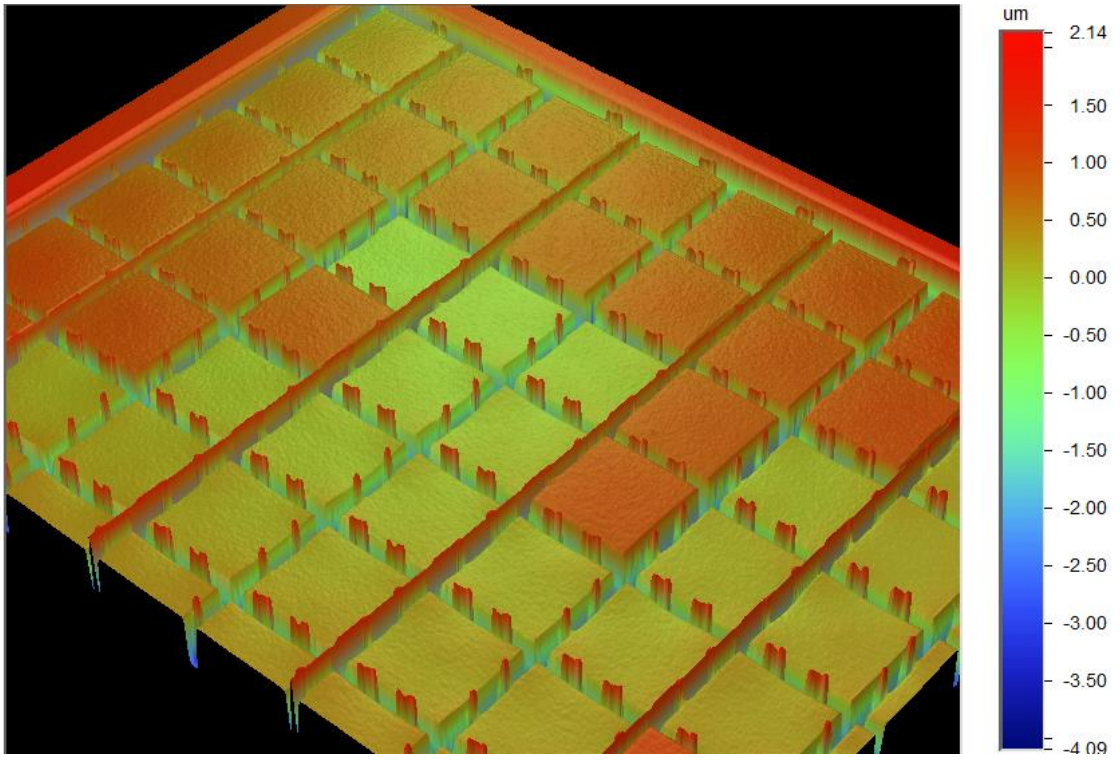

Figure 4-10: One-quarter of the MEMS array at 4.2 V, where 500 x 500 µm MEMS plates with 8 springs were partially pulled in

We saw that when we applied 4.2 V, higher than the measured pull in voltage for single structure, only a few mirrors in the row were partially pulled in as seen in Figure 4-10, and the rest of the mirrors were transiting from the release state to the pull-in state, which could be reason why we needed to apply higher voltage to the array than the single structure. As we increase the voltage to 9 V, we see that all the MEMS plates were completely pulled in to the substrate, as shown in Figure 4-11. Following this, when we reduce the voltage down to 0 V, the MEMS plate comes back to its original position, as shown in Figure 4-9. In the system with the glass lid the structure will move towards the glass. One of the advantages of SOI wafers is that the structure silicon is crystalline and has far less stress than deposited polysilicon or MEMS structures fabricated using silicon micromaching on silicon.

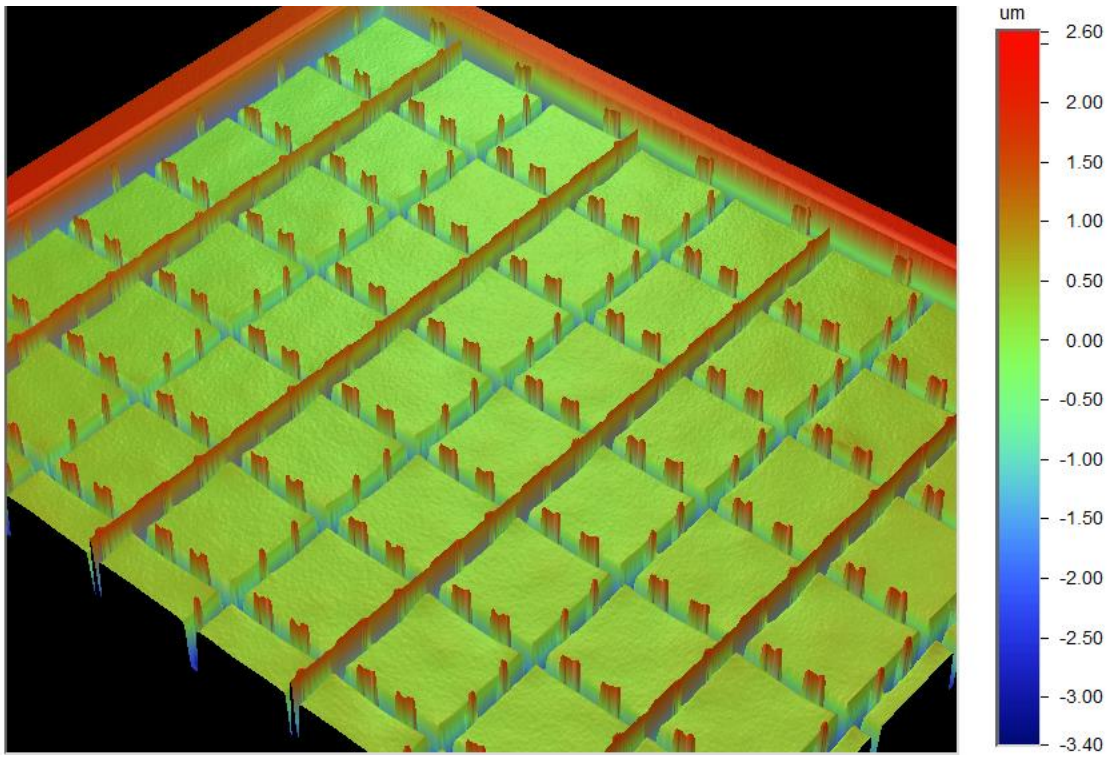

Figure 4-11: MEMS array at 9 V, where all the MEMS plate are pulled in

4.2 Bonding of the SOI Glass Chip

Since we were using a glass chip and a SOI chip, we did not want to subject the wafers to high temperature or electrical signals, as there were released structures on the SOI chip. Anodic bonding is an excellent choice of bonding for glass-silicon wafers, however it involves applying high potential (~600 V) [53], which can cause issues on the released SOI chips. Another option could be that we use diffusion bonding like Au-Au thermal compression bonding. In Au-Au thermal compression bonding, the two surfaces are bought in atomic contact, and heat and force were applied to bond the two surfaces. On both the SOI and glass wafers, 300 nm of Au is deposited and a force of 80 N at 320°C was applied for 10 minutes. One of the critical things to ensure during the thermal compression bonding was that Au was deposited at high purity. To ensure this we did a pre-sputter step before deposition of Au [33, 56].

We used a Finetech[14] PICO flip chip bonder to bond the SOI and glass lid, on the flip-chip bonder, the SOI chip was laid out flat on the chuck and the glass lid on the bonding arm as an "L shape, as shown in Figure 4-12. The tool uses a laser as a source and beam splitter to illuminate both the chip and align them. During aligning the glass and SOI chip for bonding, we found that the contrast of light was low on the flip-chip bonder, so we used an external light source to ensure we were able to see the metal on both the glass and SOI chip and bond the chips. Using micrometers, the SOI chip is aligned to the glass lid on the moveable arm. Once aligned, the glass lid is bought in contact with the SOI chip and a force of 80 N is applied. Finally, the flip-chip bonder program ramps up the chuck temperature to 320°C and holds it there for 10 min to allow diffusion of gold and bond the SOI and glass lid. We were successfully able to bond both the lids with an accuracy of +/- 5 µm.

[14] Finetech Manchester NH

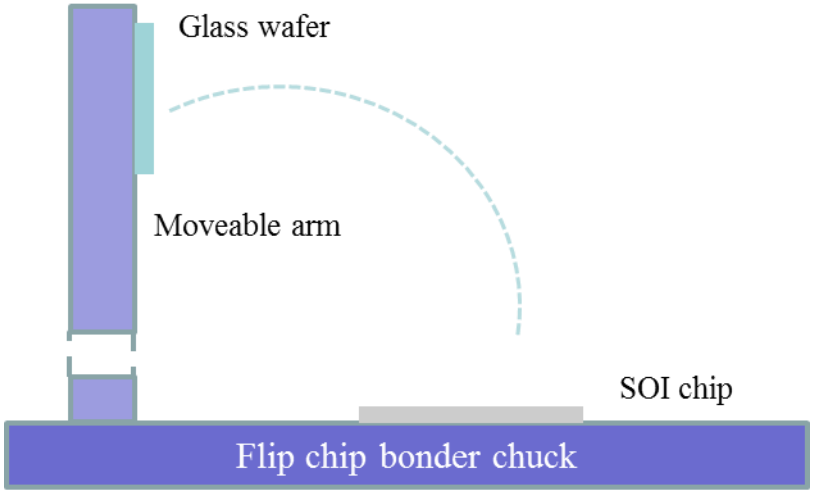

Figure 4-12: Setup for flip chip bonding of the SOI and the glass chip

4.3 PCB Mounting of MEMS Chip

Once the SOI/glass chips were bonded together, the next step was twofold. First, to rigidly bond the MEMS chip to the PCB, so that the passive CCRs could be aligned to the MEMS chip. Second, route the electrical connections of the electrodes from the bond pads on the MEMS chip to connectors on PCB using wire bonding. A 2”x2” PCB was designed with four mounting holes at the four corners to mount it with screw size #4. PCB was fabricated with electro less nickel and immersion gold (ENIG) finish, so that all the exposed solder mask area had immersion gold on them, this would allow us to do wire bonding between the MEMS chip and PCB pads. The bond pads on the PCB were made large so that we could easily wire-bond it multiple times, if needed. A chip area of 8 x 10 mm after dicing, with three pads was laid out on the PCB for the MEMS chip, the three pads on the PCB were wire bonded to the three electrodes (structure, substrate and ITO) on MEMS chip. PCB also contained some resistive protection components and connectors for connection to the sensor board. The board has three 10 kΩ in line series resistors to the electrodes and two 1 MΩ resistors between the structure-substrate and ITO-substrate electrode to prevent electrostatic discharge damage. This inexpensive board helps us

facilitate, assemble, and quickly test the working of the MEMS structure. Once the MEMS chip was fabricated and tested, the chip was then glued on the PCB in the area for SOI /glass using 5-min-set epoxy. Once the epoxy was set and chip glued to the PCB, we then use K&S 4524 wire bonder to make Au wire connection between the bond pads on the MEMS chip to the bond pads on the PCB. We made multiple wire bond connections for each electrode, to ensure that the electrodes were connected. Once that was done we used a 5 min epoxy to just fill and set in the wire bond connections. For understanding the dimensions, we in Figure 4-13 have a quarter dollar coin next to the bonded MEMS chip on the PCB.

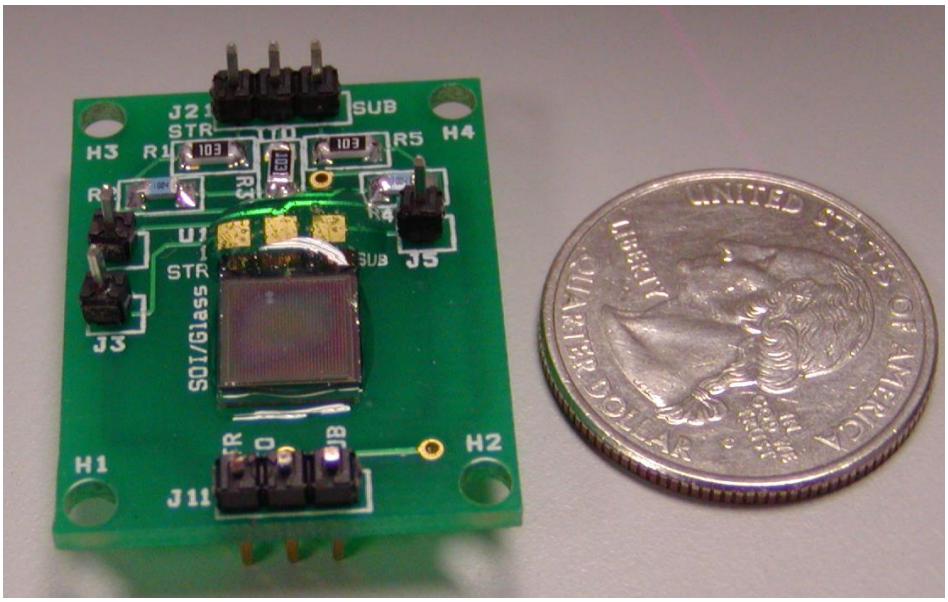

Figure 4-13: Bonded MEMS chip on the PCB

4.4 Michelson Interferometry

Once the MEMS chip was mounted on a PCB, the next step was to precisely bond the BK-7 CCR to the MEMS chip. For bonding the CCR-SOI/glass chip we used a UV epoxy that can be cured by exposing it to UV. We accurately aligned the CCR-SOI/glass chip using the principle of Michelson interferometry. In the Michelson interferometer setup [40], a collimated coherent incident laser beam is split into two arms using a beam splitter. One arm of the beam is

retroreflected back from a known precision commercial CCR, and the other split beam is retroreflected back from the CCR that we want to bond to the SOI/glass chip. Both the retroreflected beams passed through the beam splitter, and as a result the amplitude of both beams combined and an interference pattern was seen. A block diagram of the optical setup is shown in Figure 4-14.

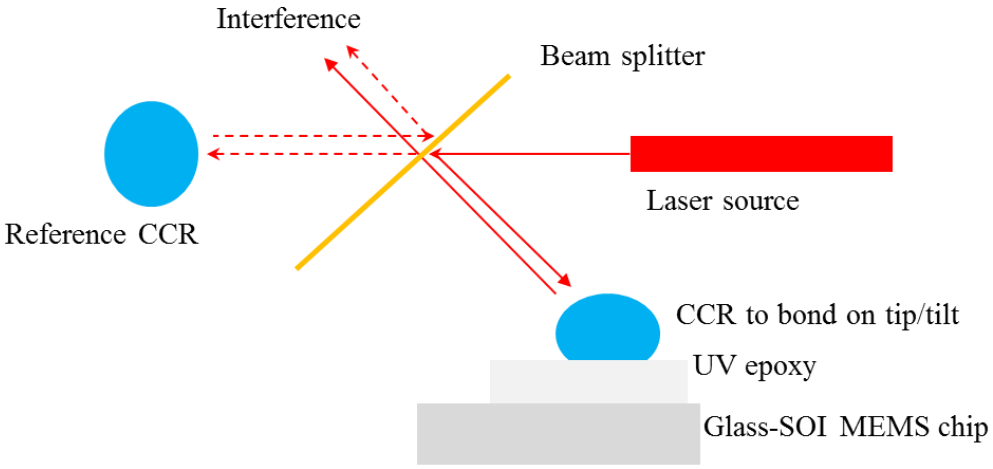

Figure 4-14: Block diagram of interferometric alignment setup for precise alignment of SOI/glass chip on PCB to CCR

To enable this experiment we developed mechanical stages to hold the CCR and provide tip/tilt and translation capabilities for aligning. Then we conducted experiments to ensure that we dispensed a minute amount of the UV epoxy to bond the CCR and SOI/glass chip, as the chip was not hermetically sealed and excess epoxy could get into the MEMS structure and make it unusable. Finally, the optical setup was put together and the SOI/glass chip- CCR was bonded. Below are more detailed descriptions of each step.

4.4.1 Mechanical Stages

A mechanical fixture was designed as shown in Figure 4-15 to rigidly hold the PCB on which the SOI/glass chip was mounted. An aluminum plate approximately ¼ inch thick was selected, and as the PCB had four 4-40 holes, four tapped holes were drilled on the aluminum

plate to screw the PCB. We made four additional holes at 2-inch spacing horizontally and 1-inch spacing vertically so that the aluminum plate could be mounted to the optical table.

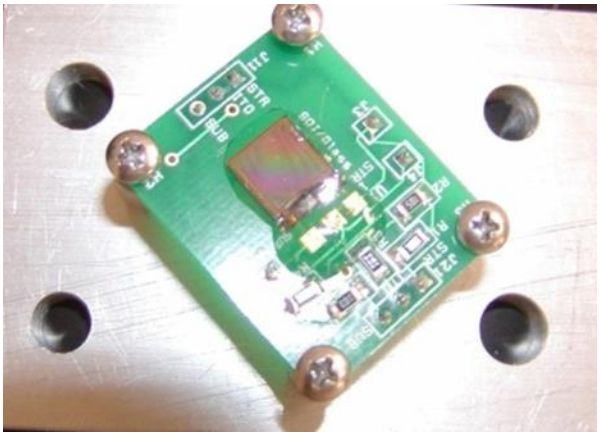

Figure 4-15: Aluminum plate to hold the SOI/glass chip PCB

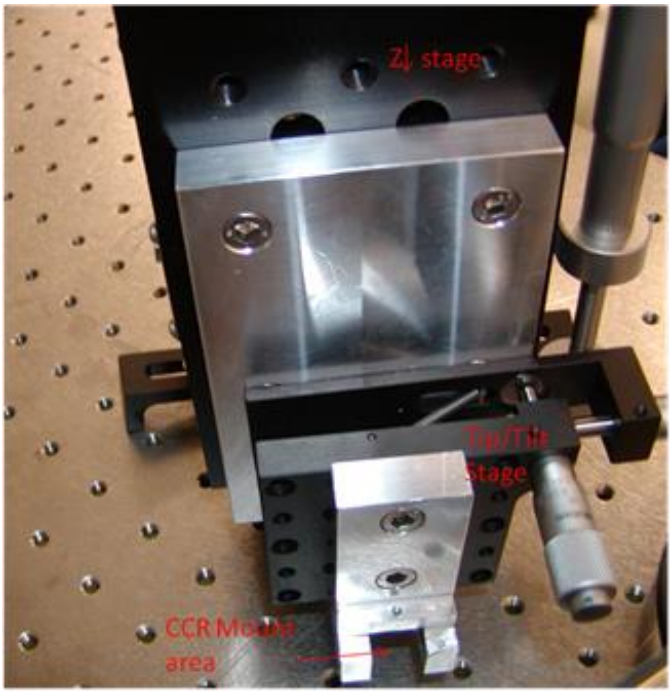

Figure 4-16: Mechanical fixture to mount the CCR and provide tip/tilt and translation using micrometers

We designed another set of mechanical fixtures to hold and allow 3D manipulation of the CCR during precision interferometric alignment to the MEMS chip/PCB as shown in Figure 4-16. The fixture allowed the CCR to be lowered using the Z-translation stage, a precision tip-tilt

stage utilized to planarize the ITO-coated glass surface with the CCR glass face to within 10 arc-seconds using an interference pattern. The CCR was mounted and held using two Nylon-tipped set screws on the side. These mechanical fixtures allowed us to rigidly place the SOI/glass PCB under the CCR, mount and hold the CCR above the SOI/glass PCB, and then lower it down and align it. The next path was to ensure that we dispensed a minute amount of UV epoxy, just enough so that it bonded without seeping into the SOI/glass chip during alignment.

4.4.2 Dispensing Experiment

A small layer of UV-cure epoxy (Norland[15] NOA 61, viscosity 300 cps) with refractive index of 1.56 at 632 nm was used to bond SOI/glass chips to CCRs. Since we wanted a thin layer of epoxy completely filling but not extruding far from the CCR-chip region, we conducted initial experiments to dispense a small amount of water (viscosity = 1 cps) to determine expected distribution. Since the SOI/glass chip was not hermetically bonded, if the UV-epoxy overflowed it could have entered the SOI/glass chip and affected the MEMS structures. We also wanted the UV epoxy to spread uniformly at a uniform thickness with no air bubbles. For our initial experiments, we used two glass slides as surfaces to bond and used dispensers ranging from 0.5 µl to 5 µl to deliver the optimum amount of liquid. We used water for our dispensing experiment, as water is non-destructive, easy to work with and safe to handle. In the experiment, the water was first pulled into the dispenser tube, then force was slowly applied to release a drop of water. Figure 4-17 illustrates the need to dispense the drop with care. Drops 1 and 3 were dispensed with the tip close to the sample, and drop 2 was dispensed with the tip pulled away from the glass surface. We found that the surface tension forces caused an undesirable increase in the volume of the liquid. After dispensing the water droplets, we placed a glass slide on top of

[15] Norland Products, Cranbury, NJ

the first slide (no force applied) to see the area covered by the drop as shown in Figure 4-18. It can be seen that there are still air bubbles between the glass slides as we applied force, the air bubble went away. We concluded that in our experiment, to ensure that there were no air bubbles in UV epoxy, we will need to apply some force from CCR side on the SOI/glass chip.

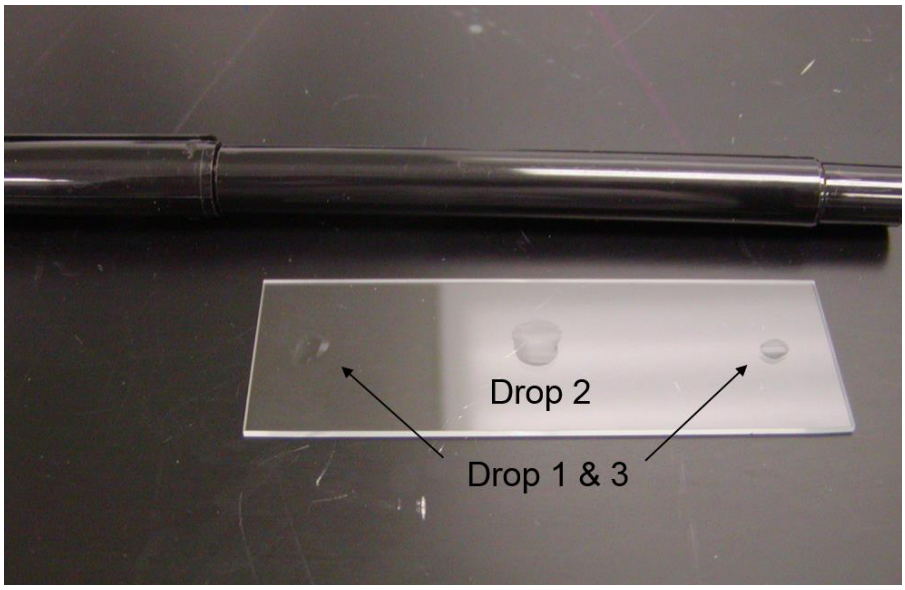

Figure 4-17: Dispensing water to understand the amount of liquid needed to ensure no spillage

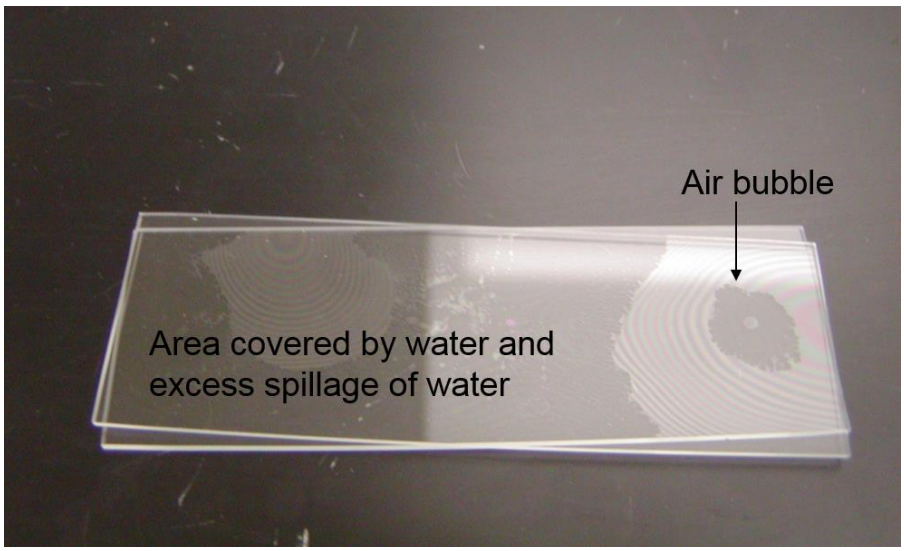

Figure 4-18: Applying no force to see if air bubbles were formed

4.4.3 Optical Set Up

The principle and working of the Michelson interferometry is explained earlier. In our experiment the Michelson interferometry setup was used to align and bond the CCR with the SOI/glass chip using UV epoxy. The block diagram of our experiment is shown in Figure 4-14, and the actual setup is shown in Figure 4-19.

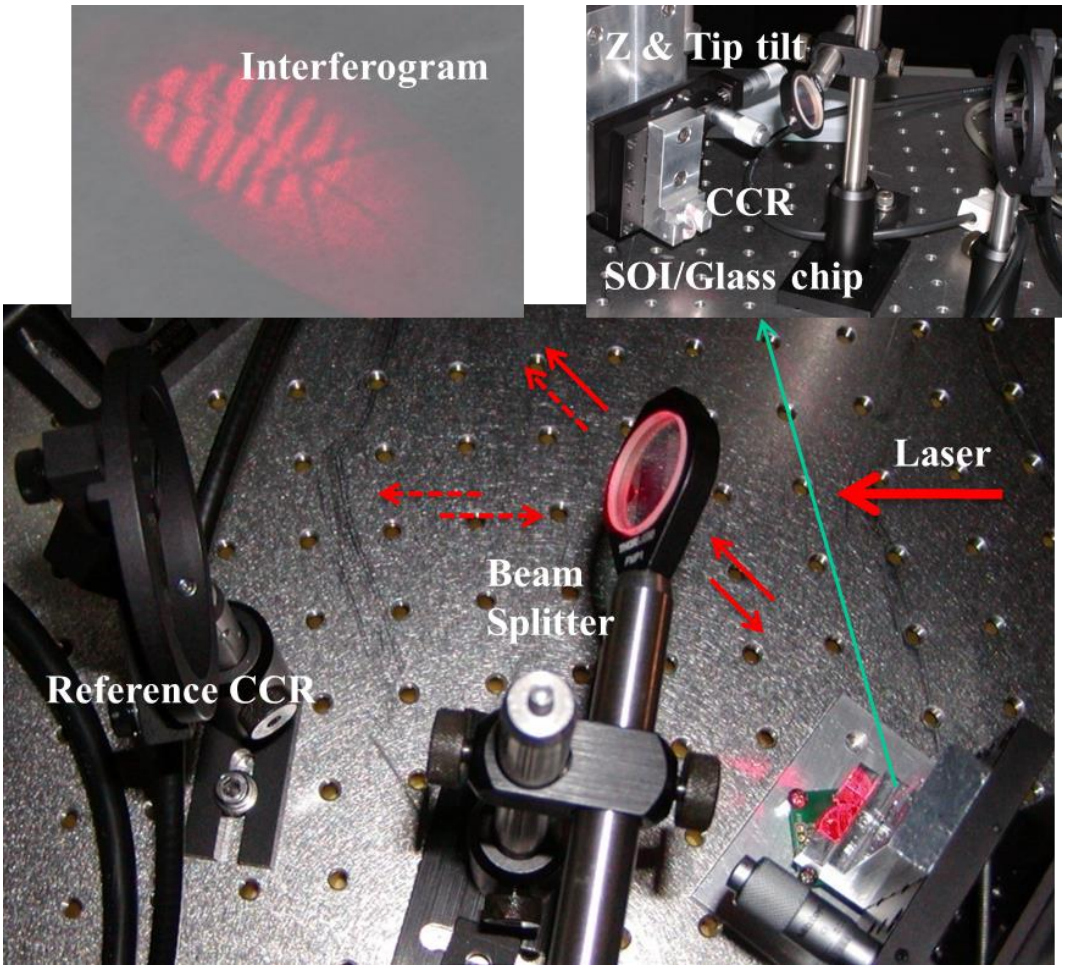

Figure 4-19: Image of optical setup of CCR and MEMS chip assembly, with a demonstrated accuracy of 20-30 arc second. Inset shows an interferogram taken during fine alignment of the MEMS chip and glass CCR.

In our experiment, we used an expanded 632.8 nm red HeNe laser as the source. As shown in Figure 4-19, the beam splitter was tilted ~70° so that one part of the beam could go straight to one reference arm of a Michelson interferometer with a precision CCR (misalignment

within 3 arc seconds). The other arm had the CCR-SOI/glass module being aligned (with UV-cure epoxy between the CCR and glass chip). When the retroreflected beams from both arms recombined, any angular deviation between the test device and the reference device produced holographic interference fringes. Once we were able to see one uniform fringe then the test device and reference device was aligned.

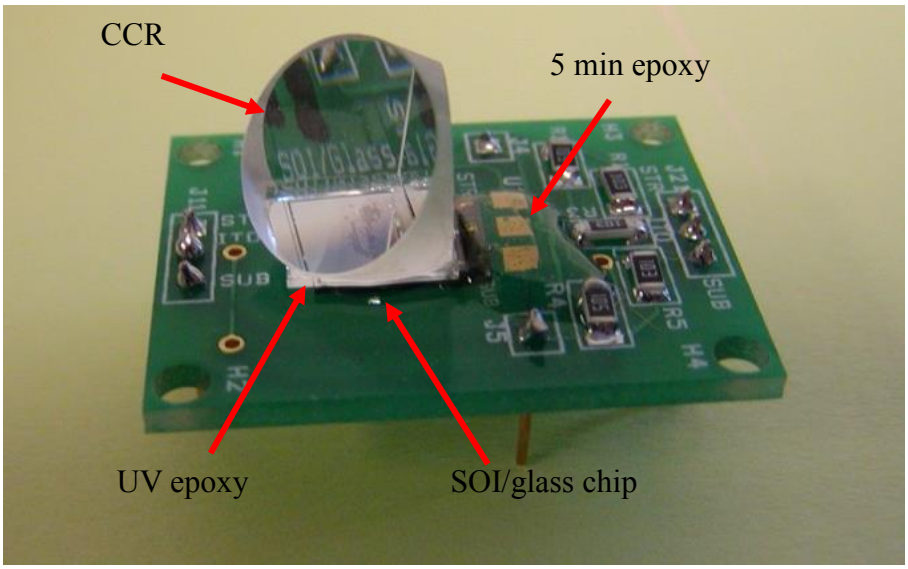

Figure 4-20: CCR aligned bonded using UV epoxy and SOI/glass chip electrodes wire-bonded to PCB and strengthened by 5 min epoxy

In our experiment, the mechanical fixture held the CCR and a few drops of UV epoxy were dispensed on the SOI/glass chip. As the fixture CCR was lowered slowly using the Z-translation stage, the liquid epoxy between the CCR and glass chip began to uniformly spread across the CCR surface. The tip/tilt stage and the Z translation stage were then slightly adjusted so that the CCR was aligned to the part as accurately as possible (i.e., when the number of fringes was minimized). A fringe pattern before final alignment is shown as the interferogram inset in Figure 4-19. We were able to align to within two to three fringes (20 to 30 arc-seconds), possibly being limited by slight bowing of the glass surface following the previous flip-chip bond step, where the glass and MEMS SOI part were mated. After this we exposed the aligned

CCR, in situ, with a UV source. The UV light was turned on for 2 minutes to cure the epoxy, and then the PCB containing the MEMS chip precisely bonded to the TIR CCR using UV epoxy was removed from the set up and is shown in Figure 4-20. Going forward, we will refer to the bonded CCR with SOI/glass chip on the PCB board as the CCR PCB.

4.5 Bench Top CCR Modulation Testing

The next experiment was to test the CCR PCB by electrostatically actuating the MEMS structure and looking at the retroreflective optical signal. First we measured the reflectivity of an unbonded commercial CCR and saw that 92% of the signal was retroreflected and the remaining 8% was lost in absorption, roughness of mirrors, scattering, and other optical properties. When we measured the retroreflectivity from a bonded CCR, the retroreflected signal was between 73%-92%. We believe some of the MEMS mirrors were either stuck to the glass chip or were in close proximity and were disrupting the retroreflected signal, already. Following this, a benchtop interrogating setup was developed to test the modulation of the bonded CCR.

One of the CCRs was crudely bonded with higher misalignment to allow us to capture the retroreflected signal easily on the benchtop setup. In the setup shown in Figure 4-21, a HeNe laser (632.8 nm) passed partially (50%) through a beam splitter and proceeded toward the CCR module. The retroreflected beam passed back into the beam splitter, which redirected 50% of that light toward a collecting lens and photodetector. A matched red optical filter was placed in front of the detector to filter out ambient light sources in the room, and the output of the detector was connected to an oscilloscope to measure the change in retroreflected signal.

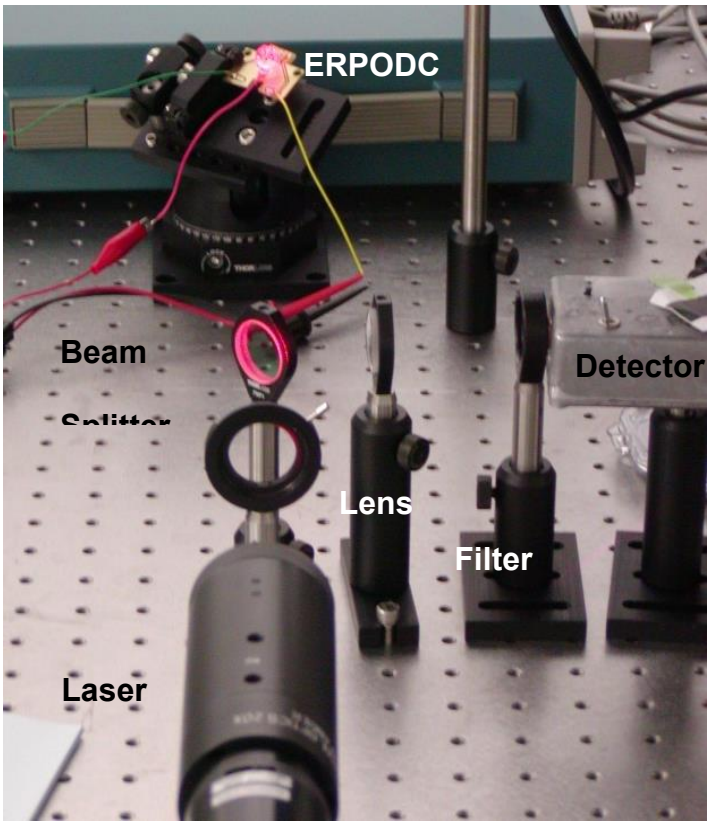

Figure 4-21: Benchtop CCR functionality testing

A DC electric potential was applied to the substrate (6 V), AC voltage was applied to the structure (0 to 6 V, at 200 Hz), and the ITO electrode was grounded. Both the applied input signal on the structure electrode and the output of the detector were viewed on the oscilloscope. An 8-12% change in modulated signal was observed, as may be seen in Figure 4-22. The bottom trace (blue) was the input signal applied to the MEMS structures, and the top trace (yellow) was the retroreflected light intensity detected by the photodetector. As we applied the 6 V on the structure electrode, the MEMS structure moved towards the ITO electrode and caused scattering of the evanescent waves, and thus the retroreflected signal during that time was 8-12% lower. As we applied 0 V on the structure electrode, the MEMS structure moved away from the ITO electrode and toward the substrate, causing less scattering, and thus during that time frame the optical signal was higher.

This benchtop experiment confirms our concept that upon actuation of the MEMS structure there was scattering caused at the glass-CCR interface, which reduces the intensity of the retroreflected beam.

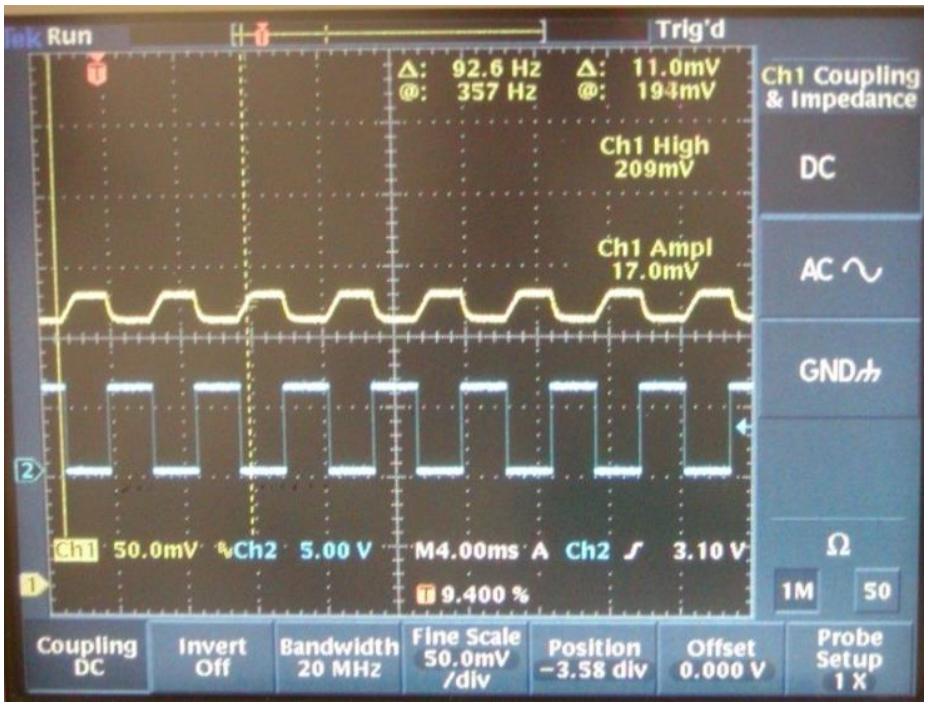

Figure 4-22: Modulation signal to the CCR (bottom trace in blue) and the retroreflected signal from the CCR (top trace in yellow).

Once the retroreflected concept was proven, the next step was to develop a sensor board that mates to the CCR board. The sensor board would provide real-time sensor data and a microprocessor to infer the data and provide actuation voltage to the CCR. This whole unit combined (sensor and CCR board) acts as the transmitter in a communication system.

The next chapter discusses the development of sensor board development of the receiver unit that contains the source, optical filtering, and electronics for decoding the modulated signal from the CCR. Following this is a discussion of the improvement made in the fabrication of the MEMS structure and further development of the receiver unit to make it compact and portable.

CHAPTER 5

DEVELOPMENT OF TRANSMITTER AND RECEIVER UNIT AND IMPROVEMENT IN MEMS STRUCTURES

Chapter 4 discussed the key aspects of the project: testing and bonding the MEMS chip and performing short-range communication. The next step, discussed in this chapter, was the development of the sensor board to complete the transmitter unit, both the CCR and sensor PCB were then encapsulated in a waterproof box. A benchtop receiver unit for immediate testing was developed. Scattering efficiency of the MEMS structures were improved using chemical etching, improvements in the receiver unit to make it portable and compact and finally long range optical communication was performed and the results were discussed.

5.1 Development of Transmitter Unit

A 2.2 square-inch sensor PCB module was developed, consisting of a low power PIC microcontroller; temperature, humidity and magnetic sensors; ½-AA 3 V Li cell, and a remote-control infrared receiver module for future data reception (Figure 5-1). Most of the components selected for the board were surface mounted, to make the entire unit compact and lightweight. We selected the ½ AA Li cell, which is not as common as AA or AAA batteries, due to weight and size advantages.

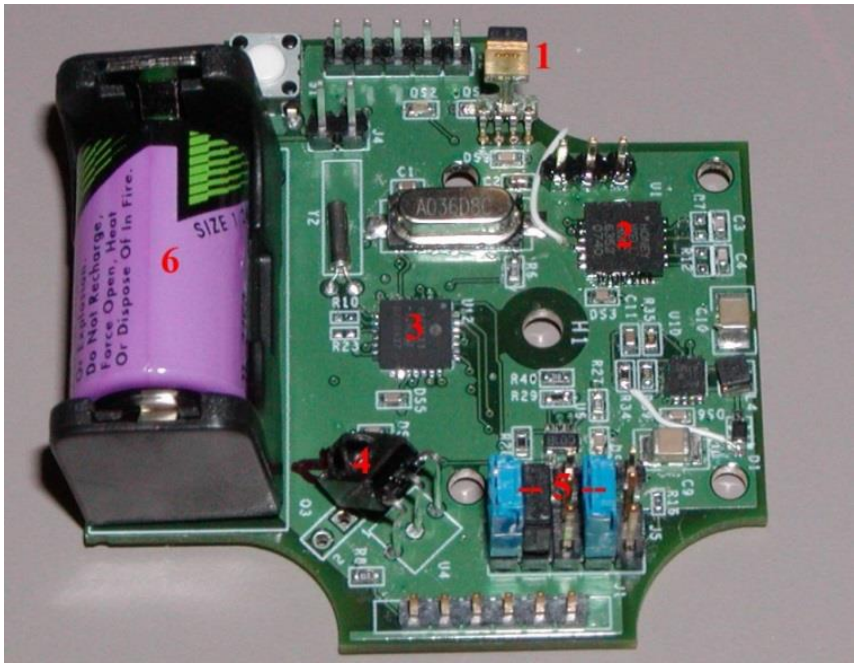

Figure 5-1: Assembled, functional sensor board. 1: temperature/humidity sensor. 2: 2-axis magnetic sensor. 3: microcontroller. 4: infrared remote control receiver. 5: field configurable jumpers.

To demonstrate sensor communication we selected off the shelf sensors. An in-house MEMS-based sensor would enable further reductions in the board size. Apart from this, several features on the board, such as headers and connectors specifically for testing purposes, can be reduced in a specific application, and the board can be made even more compact. The board has connectors for housing and communicating with the CCR module. The embedded PIC-microcontroller code (designed by me and implemented by of our software engineer Lawrence Back) periodically samples the sensors (2-dimensional magnetic, temperature, and an optional humidity sensor), determines temporal variations in the magnetic readings, and prepares and sends a data message containing the sensor and anomaly values in selectable amplitude- or phase-modulated format to the CCR board. The microcontroller has user-programmable baud rate, modulating carrier frequency, and CCR drive voltage. A debug application has been developed to verify functionality of the data packet via a hard-wired cable attachment to an

external computer. This application also allows software reconfiguration of the various transmitter options, which were field-selected with jumpers on the board. This reconfiguration ability will support a variety of CCR units and transmission ranges during system-level testing.

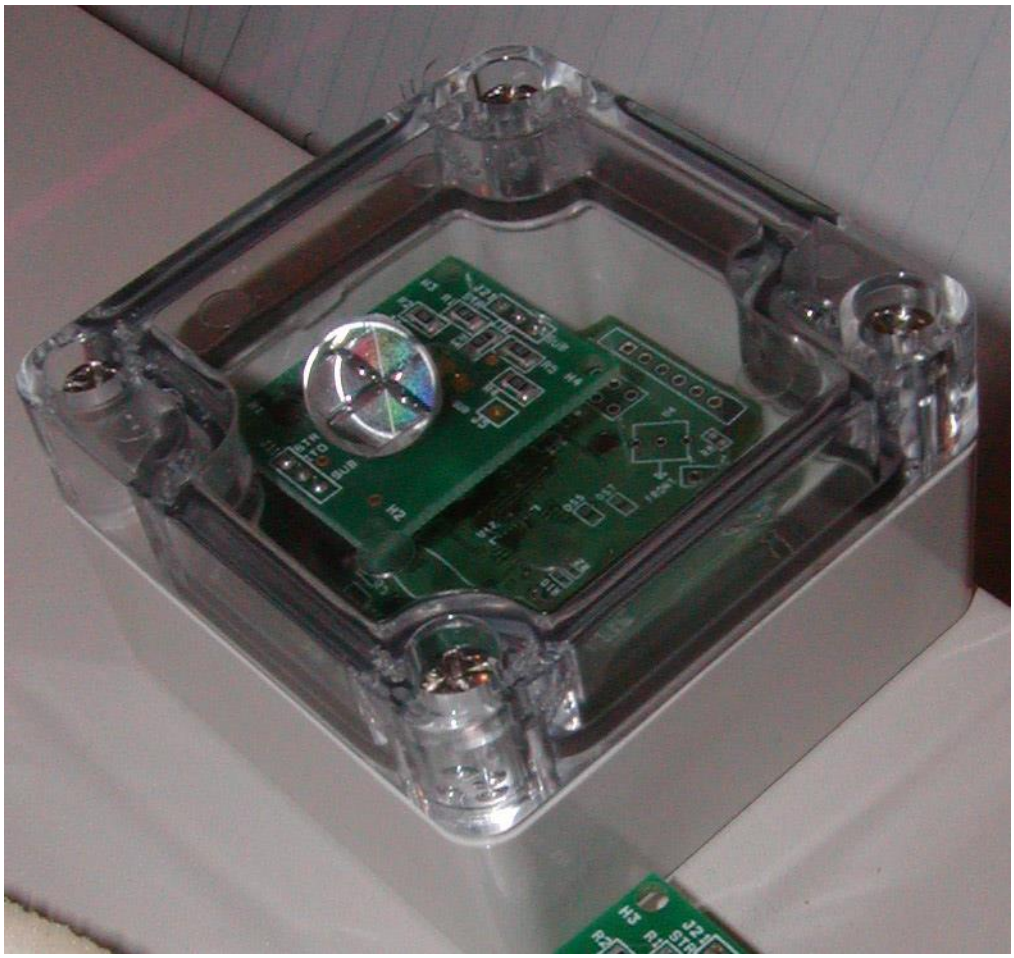

Figure 5-2: Complete transmitter unit packaged with the CCR board and the sensor board.

The sensor and the CCR board were mounted to make the entire transmitter unit and the entire unit was enclosed in a waterproof package with a transparent acrylic cover as shown in Figure 5-2, allowing the transmitter unit to be deployed in a variety of environments. The entire packaged transmitter unit weighs approximately 76 g: 5 g for the glass CCR and the MEMS chip PCB assembly, and the remainder for sensor, PCB mounting, standoffs, and battery.

5.2 Receiver Prototype Unit

The receiver unit in the communication system consists of the optical source, a laser; the optical detection unit, which consists of an optical lens to collect retroreflected signal, the optical filter, detector; and the electronics and instrumentations to process and observe the signal. Although the size of the receiver unit is not critical, making it compact and portable will help installing the receiver on UAVs or other vehicles.

A prototype receiver was rapidly developed in the lab with the available COTS and test instrumentation as shown in Figure 5-3. Most of the optical components were placed on a breadboard and attached to a tripod to allow us to easily point the laser to the transmitter unit and receive the data. The current set up was designed for both baseband (5 Hz) and high-speed (to 400 Hz) communication. Later, this chapter includes a discussion about improvements in the receiver that will enhance field deployment.

A low-power, 2.4 mW, diode laser, 635 nm from Lasiris[16] was selected as the source. The laser was externally modulated at 10 kHz to assist with separating the retroreflective signal from the ambient noise. To detect the location of the transmitter from long range, a high-sensitivity camera from Watec[17] with a 28 to 200 mm zoom lens and an LCD monitor was set up. Once the laser was turned on and the camera spotted the retroreflected signal, the signal was captured using both 25 and 150 mm collecting lenses. The reason why we had two different collecting lens, was because in one case we had expanded the beam, so that there is little beam divergence and we can collect the retroreflected signal with 25 mm collecting lens. On the other we had not used a beam expanded and used a 150 mm collecting lens. We found that that the 150 mm

[16] Coherent, Santa Clara, CA
[17] Watec, Japan

collecting lens worked better than the 25 mm lens concept. The collected signal was then filtered through a band pass filter (BPF) to reject ambient light sources away from the laser wavelength.

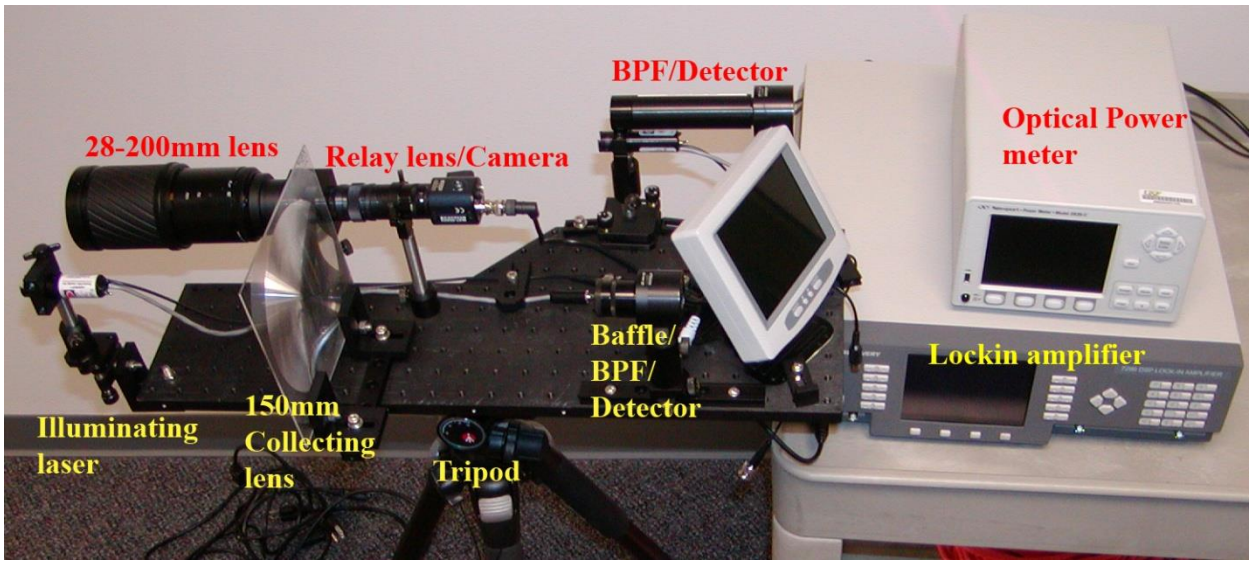

Figure 5-3: Prototype receiver with baseband and high speed communication using COTS and test instrumentations.

The detector and the electronics to process the signal were next to the BPF. For detection, we used Newport's visible photodiode (918D) and an optical power meter (2935C) [57], whose output was sent to a Tektronix[18] oscilloscope (TDS3032) and/or lock-in amplifier (Signal Recovery[19] model 7280). The lock-in amplifier and oscilloscope allowed us to test and visualize both the laser modulation and the transmitter unit amplitude modulation (AM) or phase-shift keyed (PSK) communication protocols without having to spend hours designing and testing multiple custom PCBs. Although this receiver unit was not very portable, using the oscilloscope and lock-in-amplifier helped us understand and debug the retroreflected signal. While improvements in the receiver unit's portability were implemented, outside testing was performed

[18] Tektronics, Beaverton, OR
[19] Signal Recovery, Oak Ridge, TN

using the CCR unit to understand how long we can communicate and how to elongate the range of communication.

5.3 Testing Optical Communication

Once the prototype receiver and a transmitter unit were implemented, we began testing the optical communication between the transmitter and receiver. One of the first steps in optical testing was to check if we could spot the CCR at a long distance. The next step was to using phase-shift keying or amplitude-shift keying modulation technique on transmitter to enable optical communication and detection.

5.3.1 Precision Bonding Conformation

We first verified that the precision bond alignment was highly accurate to at least 0.1 mrad (30 arc second). The receiver unit was set up at a higher elevation in a parking garage in St. Petersburg, FL.

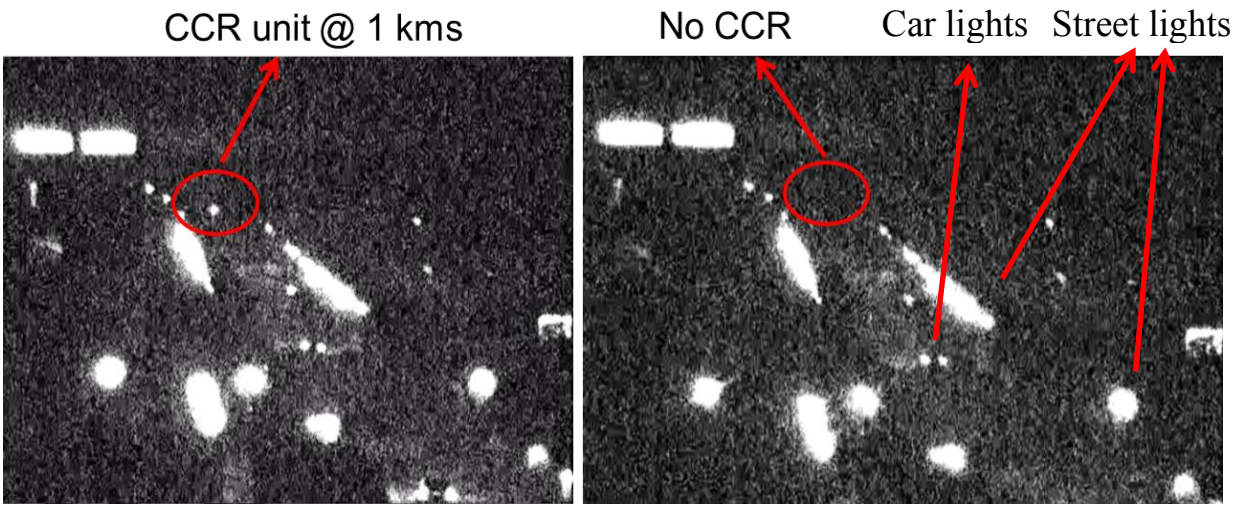

Figure 5-4: CCR unit visible from a 1.0 km range.

The transmitter unit was placed on a car and driven away from the receiver while a GPS determined the distance between the transmitter and the receiver. As seen in Figure 5-4, we could see the retroreflected light concentrically with the illuminating laser, and the transmitter

units were visible at our longest test distance (1.0 km). In fact, this high accuracy made the retroreflected laser intensity on the nearby (but not concentrically located) video camera notably less intense than next to the laser, especially at shorter ranges. Although it is not required, illumination located in line with the video camera was preferred for the best sensitivity. This test also showed that the communication channel was highly directional, a trait desirable for clandestine communication or tagging.

5.3.2 Phase Shift Keying (PSK)

On the transmitter unit, the data from the temperature, humidity, and magnetic sensor was digitized and send to the microprocessor. The microprocessor encoded the data using an electrical phase-shift method called differential phase shift keying (DPSK) [58], so that sensor data can be differentiated from the noise. The sensor data was encoded with DPSK by altering the phase of the carrier depending on the sensor bit value; the microprocessor depending on the sensor bit value applies potential to the structure electrode on the CCR PCB and that modulates the CCR unit. The receiver unit takes in the incoming retroreflected signal encoded with a DPSK scheme, which was decoded by the lock in amplifier (LIA) and displayed on an oscilloscope. We used the LIA as a tuned phase discriminator and the oscilloscope and human observer as the decoder.

The transmitter used a 400 Hz carrier frequency and a 5 bit/second data rate. The LIA oscillator frequency was set to 400 Hz. However, using the LIA allowed us to tune into a particular frequency at which we could differentiate the retroreflected signal from noise. The DPSK scheme had a qualitatively higher (better) signal to noise (SNR) ratio compared to the amplitude shift keying scheme that was also tested. A precise SNR measurement was not performed due to limited resources.

5.3.3 Long Range Communication

By using a 635 nm laser as an interrogating laser at the receiver end at a communication distance of 56 m, (Figure 5-5), we observed the retroreflected signal with both amplitude and phase shift keying techniques. We ensured that the laser light was focused on the retroreflector. At a close distance, if the laser were not focused, we did not receive the retroreflected signal. To focus the laser, we used an Energizer MLT3W2AAL, 3-W LED flashlight to spot the transmitter unit, and focused the laser on the transmitter unit. As we increased the distance, we found that at around 120 m, we could see communication between the low-speed (5 baud) data and the transmitter unit and the lock-in amplifier using a PSK modulation protocol (400 Hz carrier frequency), but not with amplitude shift keying. Video decoding was more sensitive and would have given better response; however, video decoding of low-speed data was not possible because the modulation depth of the transmitter units was currently <10%. This was because the transmitter area on the camera was typically saturated due to the efficient retroreflection of the illumination source, and a 10% reduction still saturates the camera to roughly the same extent.

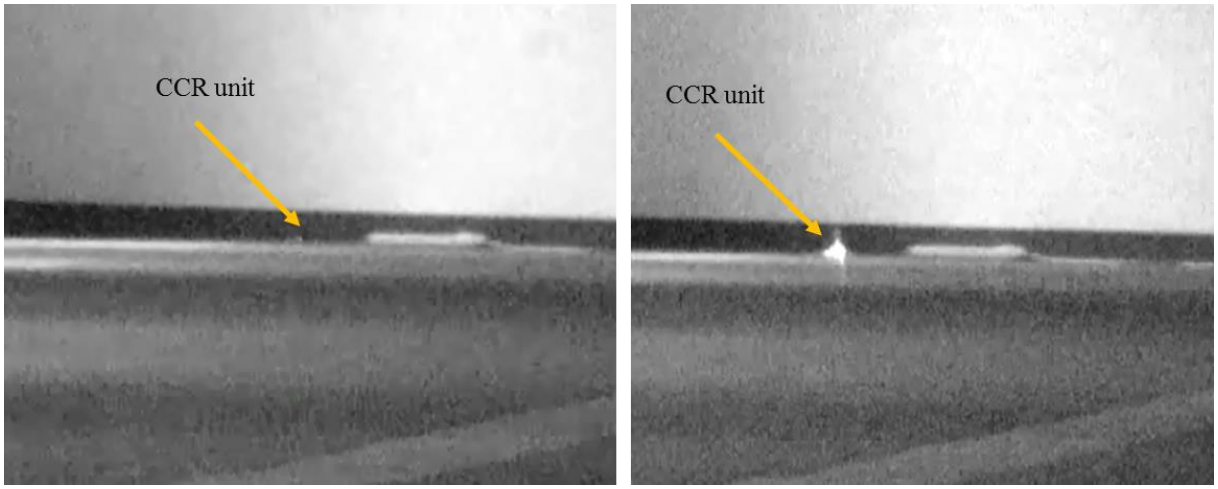

Figure 5-5: Testing at 56 m with the CCR on the ground and the view from the camera.

During testing, we used 5 baud speed; however, while testing under an optical profilometer, we found that the MEMS structures can be modulated up to 18 kHz, so high-

frequency communication is possible. We could communicate at around 120 m using PSK, but not beyond that range; however, we identified several improvements that can be made both to the MEMS structure (and transmitter) and the receiver to extend the range of communication. The next section discusses these improvements.

5.4 Improvements in MEMS Structures

We revisited the fabrication of the MEMS structures and developed a method to improve the scattering efficiency. On the MEMS plate, the release holes help release the plate and increase scattering by interacting with evanescent waves at the glass-silicon interface. We could improve the scattering efficiency by introducing roughness on the smooth SOI surface. The roughness should ensure that most of the structure's silicon interacts with the evanescent waves, which decay approximately 200 nm from the surface of the glass-silicon interface. Fabricating the MEMS structures with polysilicon as oppose to single crystal silicon, would increase roughness as polysilicon is a little rougher, however intrinsic stress of polysilicon can cause the structures to bow after release. To produce scattering features or roughness, we conducted following experiments on both silicon and polysilicon chips and considered incorporating the following additional processes in final fabrication:

- Mechanical abrasion
- Multiple exposures of the photomask
- Plasma etching
- Isotropic and anisotropic wet etching
- Polysilicon as structure material instead of silicon

The optical reflectivity from the processed silicon and polysilicon test samples were measured, and compared to a bare silicon wafer. In the testing, a roughed sample was placed

vertically on the sample holder, and the laser beam was introduced at 45° angle. The reflected beam goes through the filter to the optical power meter. During experiments, all the ambient light sources, except the laser, were turned off. To ensure a consistent reading, the power meter reading was set to zero to eliminate all the dark current before we turned on the laser. The setup of the experiment is shown in Figure 5-6.

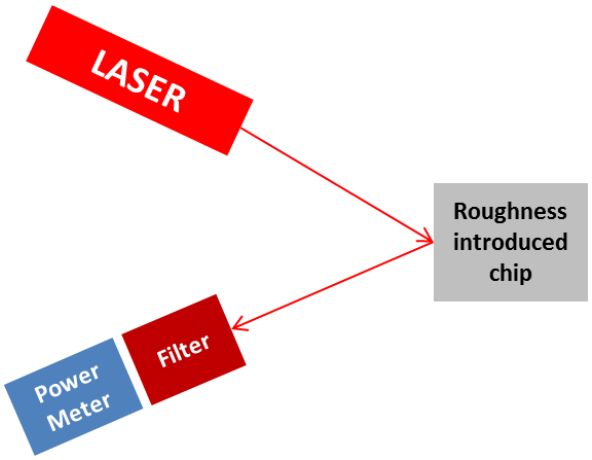

Figure 5-6: Set up for reflectivity test of a roughness-introduced chip.

5.4.1 Mechanical Abrasion

Inducing roughness by using a mechanical process is relatively simpler, but controlling the depth in nanoscale is difficult. When bead blasting and other sand paper abrasion steps were used, care was taken to ensure that the roughness was only on the surface. A piece of silicon was slowly blasted with minute glass bead. This process did roughen the smooth silicon surface, but it is not a precisely controllable process and did not produce a consistent result. Some areas were rougher than the others; a roughness variation of 14μm on the processed side was noted. Sandpaper was used to roughen the polished silicon, and the results were similar to the bead blasting method, producing uneven irregular roughness. Without providing consistency or the required control over the depth of roughness, both the mechanical abrasion processes were abandoned.

5.4.2 Multiple Exposures of the Photomask

During processing of the SOI wafers, the *structure mask* that defines the MEMS structure (plate) contains release holes and spring features these features can be deliberately misaligned and exposed multiple times to cause a more varied topographic pattern. The multiple-exposure step can be introduced after the defined structure pattern was exposed and etched into the silicon. The multiple or subsequently exposed features can be shallowly etched into the structure silicon after the initial exposure and etch without affecting the release process while allowing a more complex (efficient) optical surface.

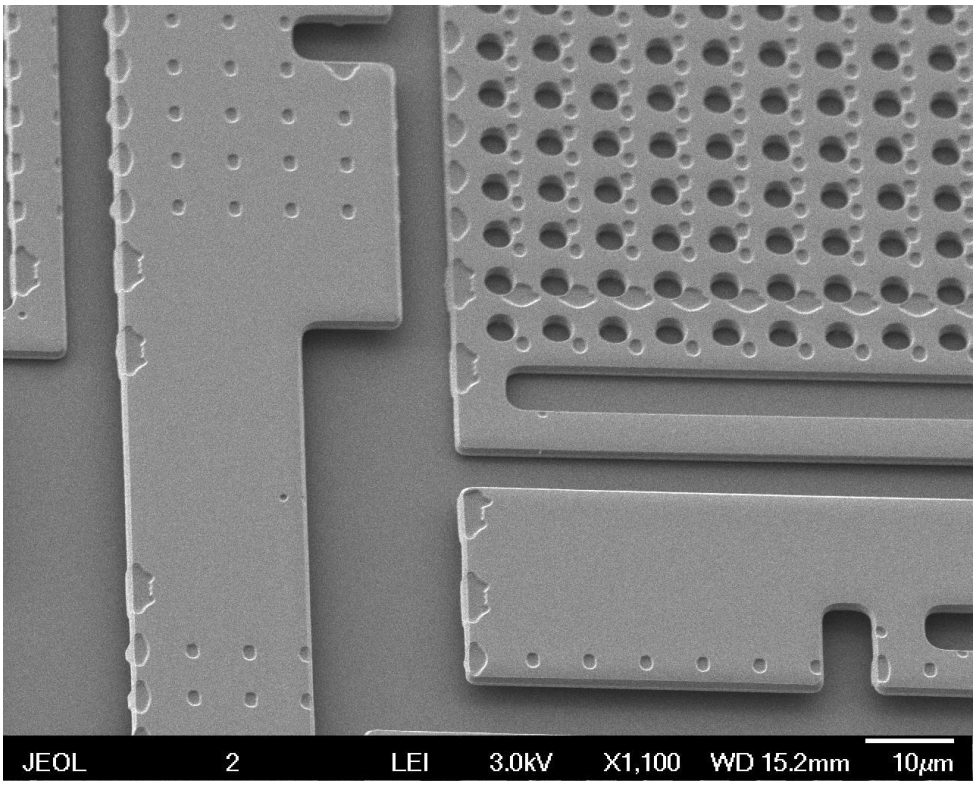

Figure 5-7: SEM image of a triple exposed SOI chip to improve scattering efficiency

Figure 5-7 provides SEM images of one such processed wafer, where the mask was exposed twice, developed and etched approximately 300-400 nanometers, and then re-patterned and etched deeply to the buried oxide layer. The triple-exposed SOI chip showed an improvement of 26% compared to the single-exposed SOI chip per the reflectivity test conducted

and tabulated in Table 5-1. An SOI wafer was fabricated using this technique, and chips from the wafers were released and used for subsequent optical communication testing.

5.4.3 Plasma Dry Etching

In plasma etching, ionized gases at high RF or DC power interact with a specimen placed on a substrate depending on the configuration of the etching tool, either a barrel or parallel plate. The plasma etching can be isotropic or anisotropic respectively [45, 55, 59]. In the semiconductor industry, isotropic plasma etchers are used to remove organic material on a nanoscale. Also, since the etching is slow, the depth or roughness created can be controlled. Isotropic plasma etching was performed in Tepla[20] using oxygen and plasma. The standard descum recipe on Tepla, *descum _300_0_0_400_xx,* and was used. This recipe used 300 sccm of O_2 at 400 W plasma power. The *xx* in the recipe denotes the etch time in minutes. Various recipes with different etch time were created, and samples of silicon and polysilicon were etched. The effect this etching had on the optical reflectivity of the surface is tabulated in Table 5-1. Along with this directional plasma etching using Unaxis, reactive ion etching (RIE) was also performed. In RIE, a recipe similar to the *descum* etch recipe was used, which had 200 W power and 50 sccm flow of sccm of oxygen. We performed varying etch times in RIE and Tepla up to 80 minutes and observed that the silicon sample seemed to become more reflective than what we started with. This could also illustrate that using an O_2 plasma cleans some inorganic contaminants and improves the surface optical properties.

In another experiment, a mixture of CF4 and O_2 gas were used in Tepla. The CF_4 etches silicon slightly and can improve the scattering efficiency of smooth single-crystal Si. The recipe used was *etch _100_0_80_400_3*, which had 100 sccm of O_2 and 80 sccm of CF_4. At etch times

[20] PVA Tepla, Corona, CA

of 5 minutes or longer, reflections as low as 6% (94% scattering) were obtained. However, these etch profiles appear to have etched the silicon very non-uniformly over the wafer surface. We tried to perform the same experiment in the RIE tool, but were unable to control the etch depth. Results are summarized in Table 5-1.

Table 5-1: Summary of optical reflectivity from mechanical and plasma processed samples of silicon and polysilicon-coated silicon.

Sample type	Tool	Etch time in min	Estimated etch depth	Optical detector reading in µW	Ratio of optical detector to bare silicon
Silicon			0	361	1.00
Backside of SSP			Rough (3-4µm)	14.6	0.04
Silicon	Bead blasted		10-15µm	34	0.09
Silicon	Sand paper scratch			197	0.54
SOI chip	Single exposure		-	221	0.61
SOI chip	*Triple exposed*		*300-400 nm*	*125*	*0.35*
Silicon	RIE with O_2	15		358	0.99
		30		300	0.83
		45		309	0.86
		60		442	1.22
Silicon	Tepla with O_2	20		320	0.89
		40		313	0.87
		60		322	0.89
		80		361	1.00
Polysilicon	Tepla with CF_4	3		204	0.56
		5		231	0.64
		10		164	0.45
		20		23	0.06
Silicon	Tepla with CF_4	3		192	0.53
		5		224	0.62
		10		177	0.49
		20		58	0.16

5.4.4 Wet Etching

We etched silicon and polysilicon pieces with isotropic etchant (a mixture of hydrofluoric acid, nitric acid, and water or acetic acid) and anisotropic etchant (potassium hydroxide) to understand the roughening (etch) effect of silicon and polysilicon with these etchants and how roughing affects the optical properties. The results are tabulated in Table 5-2.

5.4.4.1 Isotropic Etching

Isotropic etching of single-crystal and polysilicon-coated silicon using various concentrations of HF: HNO3: H2O (HNA) was performed. We varied the concentration of hydrofluoric acid, while keeping the nitric acid and water concentrations the same. We then varied the nitric acid concentration. The concentration of water remained the same, as the literature indicates that varying the concentration of water does not affect the roughness of etching [60, 61]. Reduced HNO_3 concentrations are known to roughen silicon surfaces, but in the experiments we performed and for the short etch times, it did not cause any effect. As seen from the etch results in Table 5-2, the combination of HNA at 20:20:60 sccm yielded a rougher surface than lower nitric acid combinations, contrary to our expectations. From the literature, we found that isotropic etching forms nanopores, which can make the surface rougher [54, 62-64]. After a few experiments, when we etched the silicon chip with an HNA combination of 30:20:40, nanopores were formed at the surface of the silicon. Since etch was so rapid, it took 20-30 sec for nanopores to form on the entire silicon chip. Measuring these nanopores was very difficult using a profilometer, so we conducted an experiment in which we excited the etched silicon chip with a 442 nm He-Cd UV laser, as nanopores exhibit fluorescence when excited with a UV laser. As shown in Figure 5-8, the etched polysilicon chip shows fluorescence (in red)

when excited with a UV laser. This helps us infer that nano pores were formed at the surface of the silicon/polysilicon chip, which is also consistent with results reported in the literature.

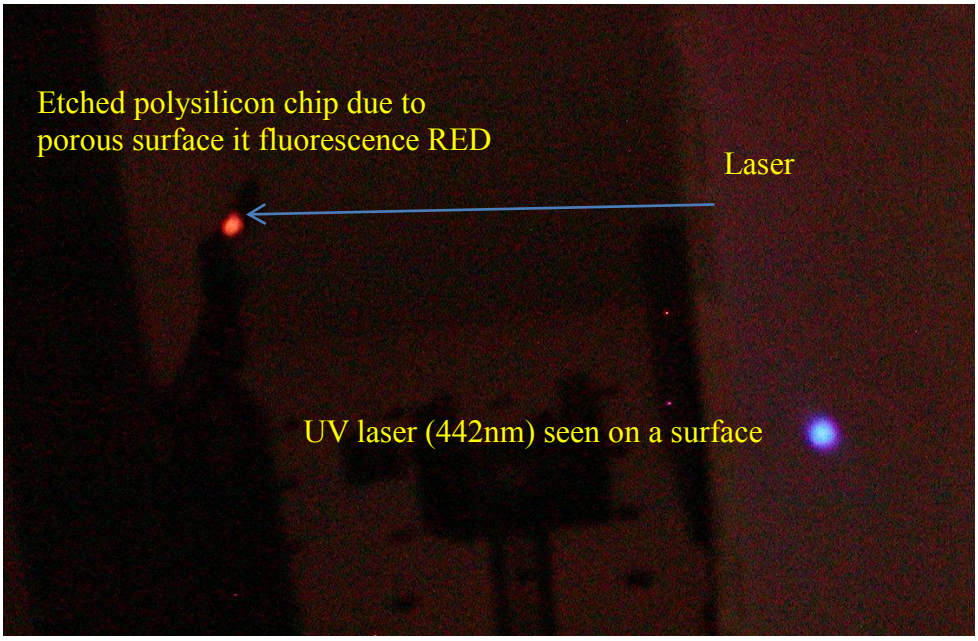

Figure 5-8: Fluorescence by nanopores when illuminated with He-Cd laser.

5.4.4.2 Anisotropic Etching

We also pursued the path of anisotropic etching of silicon. KOH is known to produce a mirror-like surface after etching silicon; however, depending upon the process conditions, literature suggests that at lower concentrations of KOH, the etching produces less smooth surface [45, 60]. We started our experiment by etching pieces of silicon and polysilicon in various concentrations (6-25%) of KOH and for different times, at temperatures from 70-75°C.

As reported in Table 5-2, the pieces etched at a 6% KOH concentration produce the best results; the reflectivity test indicates that the surface becomes rougher (<6%) as the etch goes for a for longer time (15-20 minutes). Looking under microscope and scanning the sample under a profilometer indicates good overall uniformity. However, as we etch longer, the overall etch depth increases, so integrating this process condition onto SOI wafers with only a few microns

thick structural layer is challenging. The shorter, 5-minute KOH etch also roughed the surface, lowering the optical reflectivity to approximately 40%.

Table 5-2: Summary of optical reflectivity from wet processed samples of silicon and polysilicon

Sample type	Tool	Etch time in min	Optical detector reading in µW	Ratio of optical detector to bare silicon
Silicon	HNA30:5:65	5	310	0.86
	HNA 20:5:75	5	322	0.89
	HNA 10:5:75	5	309	0.86
Polysilicon	HNA30:5:65	5	280	0.78
	HNA 20:5:75	5	310	0.86
	HNA 10:5:75	5	312	0.86
Silicon	HNA 20:20:60	5	288	0.79
	HNA 20:10:70	5	294	0.83
	HNA 20:3:78	5	300	0.85
Polysilicon	HNA 20:20:60	5	261	0.72
	HNA 20:10:60	5	332	0.91
	HNA 20:3:78	5	320	0.90
Silicon	HNA 30:20:40	0.5	20	0.06
Polysilicon	HNA 30:20:40	0.5	1	0.00
Polysilicon	KOH 6%	5	159	0.44
	KOH 6%	20	1	0.00
	KOH 15%	5	142	0.39
	KOH 15%	20	59	0.16
	KOH 25%	5	194	0.54
	KOH 25%	20	64	0.18
Silicon	KOH 6%	5	142	0.39
	KOH 6%	20	21	0.06
	KOH 15%	5	211	0.59
	KOH 15%	20	59	0.16
	KOH 25%	5	213	0.59
	KOH 25%	20	63	0.17

After comparing the reflectivity results from plasma etching and wet etching, we felt that the wet isotropic etching process gives us a good nanoscale scattering feature and, since etch time is so short, the amount of silicon etched is in the nanometer range. We finalized the isotropic etching of silicon as the best method to improve the scattering efficiency of the SOI chip and started chemically introducing roughness on the fabricated SOI chips before bonding.

Figure 5-9 shows the difference between the chemically treated SOI chip and the previously used, untreated SOI chip. Although we made significant improvement in the scattering efficiency and performed all the tests on both silicon and polysilicon, from the results shown in Table 5-2, we found that the polysilicon is rougher than silicon and would produce higher scattering.

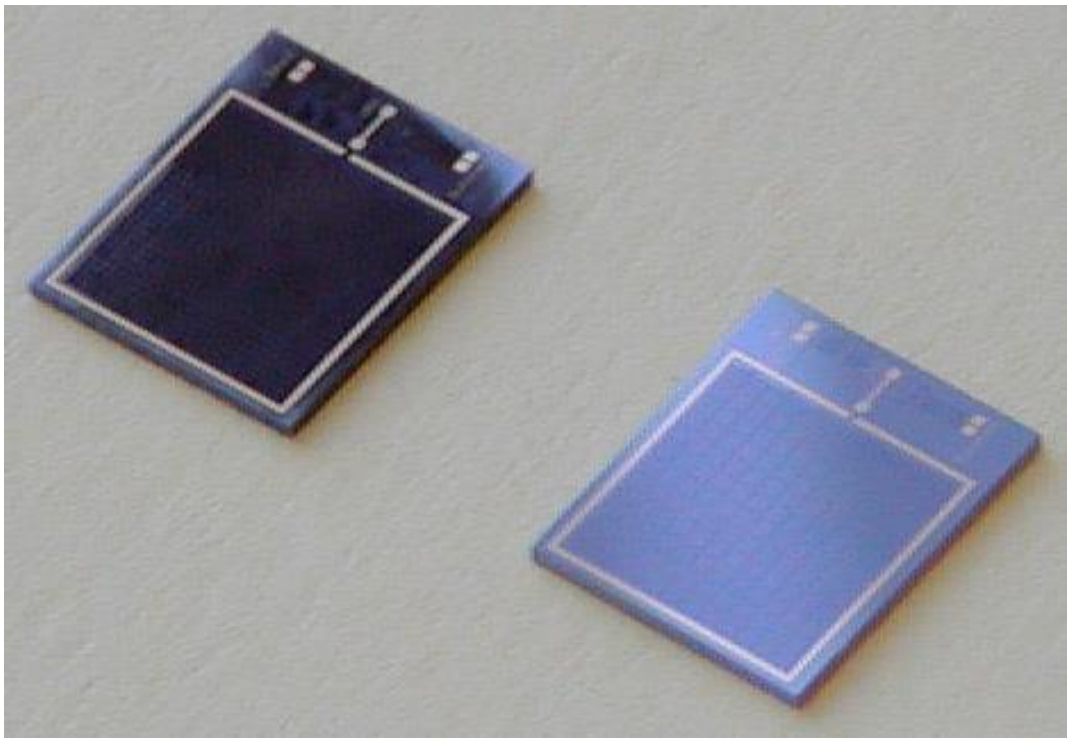

Figure 5-9: Optical image illustrating the difference between an HNA-treated chip to an untreated chip.

5.4.5 Using Polysilicon on an Insulator Wafer

All the chemical and plasma etching tests indicated that etched polysilicon was rougher than single-crystal silicon. Although we significantly increased scattering efficiency using isotropic etching on silicon, isotropic etching on a polysilicon surface yielded even higher scattering efficiency. Therefore, we prepared a polysilicon-on-insulator wafer, and processed it with the same process flow as we used for our SOI wafer. This process also had the potential to reduce the number of process steps and wafer cost significantly, as we can deposit polysilicon in-house and use economical single-side polished silicon wafer instead of costly, custom-designed

silicon-on-insulator wafers. The process was completed, the wafer was diced, and several finished chips were released in HF (1 min 50 sec) and rinsed.

The small MEMS plates (100 x 100 µm) after release had a bow of approximately 200-250 nm, and the medium MEMS plates (200 x 200 µm) had a significant bow of 600 nm. Figure 5-10 illustrates the Wyko surface profiler plot with the bow. Intrinsic stress causes excessive bow; so, although the polysilicon-on-insulator method may be economical in production, for experimental purposes, the SOI wafers made more sense.

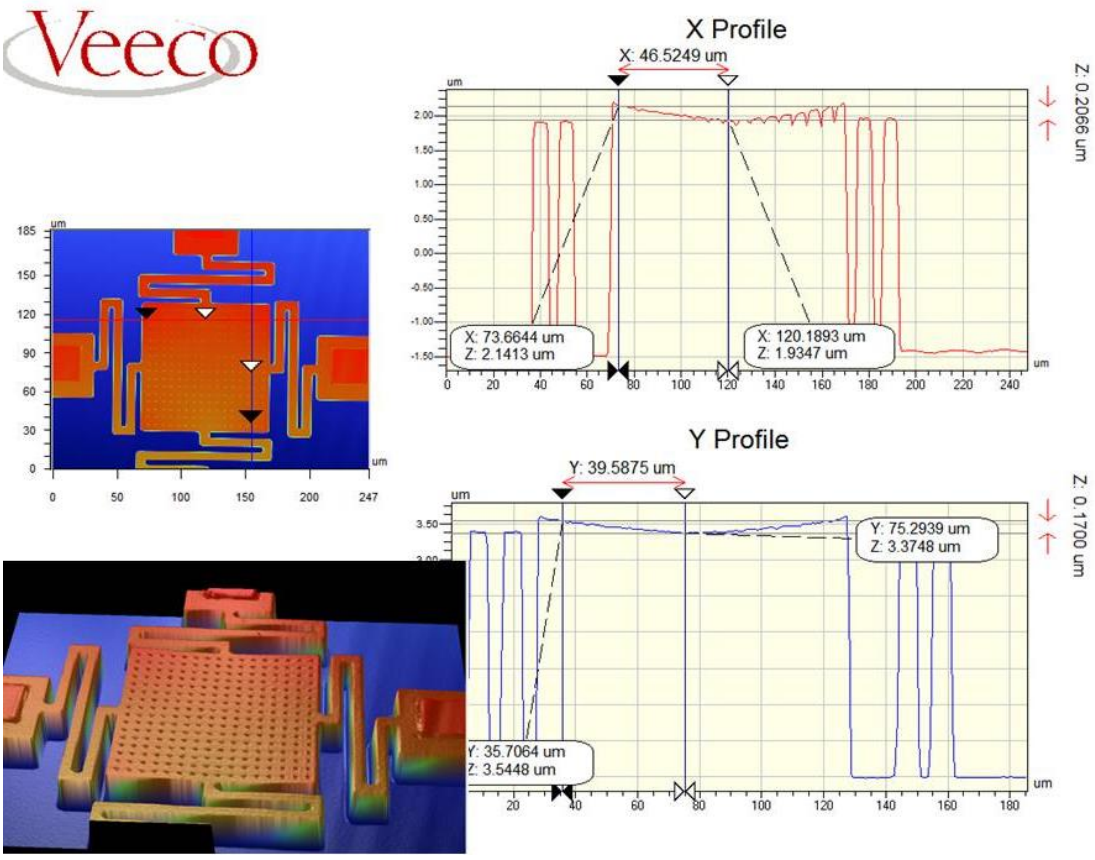

Figure 5-10: Optical profilometer data illustrating that the MEMS plate fabricated on polysilicon had significant bow after the release of mirrors due to intrinsic stress.

We ended up using HNA-etched SOI chips as the MEMS chip in the transmitter unit. We believe that the improvement in the scattering efficiency will enable longer range

communications. The next section discusses improvements in the receiver unit to make the unit more portable and better able to efficiently capture and process all the retroreflected signals.

5.5 Improvements in the Receiver Unit

The receiver unit was divided into parts, and each part was tested and improved. The receiver system was divided into four parts: a *power unit*, which connects to an external battery and delivers appropriate voltage to other components; the *laser driver unit*, which powers either a 635 nm or 980 nm wavelength CCR-interrogating diode laser; an *optical detector unit*, which detects the optical power received; and a *data detection unit*, which decodes the received data. To make the receiver unit portable and stable, the components were mounted on a tripod with optical rails. All the sections of the receiver are shown in Figure 5-11 and Figure 5-12.

The data detection unit consists of a pre-amplifier board, compact USB-based National Instruments (NI-USB 6211) data acquisition (DAQ) module, and customized LabVIEW software running on an attached laptop (not shown). The optical data collected by the detector unit goes to a pre-amplifier board, which amplifies the data and sends it to the DAQ card. The DAQ card and PC-based software digitize and decode the transmitted retroreflection signals from the noise. A laptop serves as the digital processing and display unit. It performs amplitude- or phase-demodulation used for data discrimination, and displays the received data in text or graphical format on the user's computer monitor. Because the LabVIEW program was not fully developed during the project, for experimental purposes, a Signal Recovery Model 7280 lock-in-amplifier (LIA) was used for decoding the transmitted retroreflected signal and displaying the decoded data on the oscilloscope.

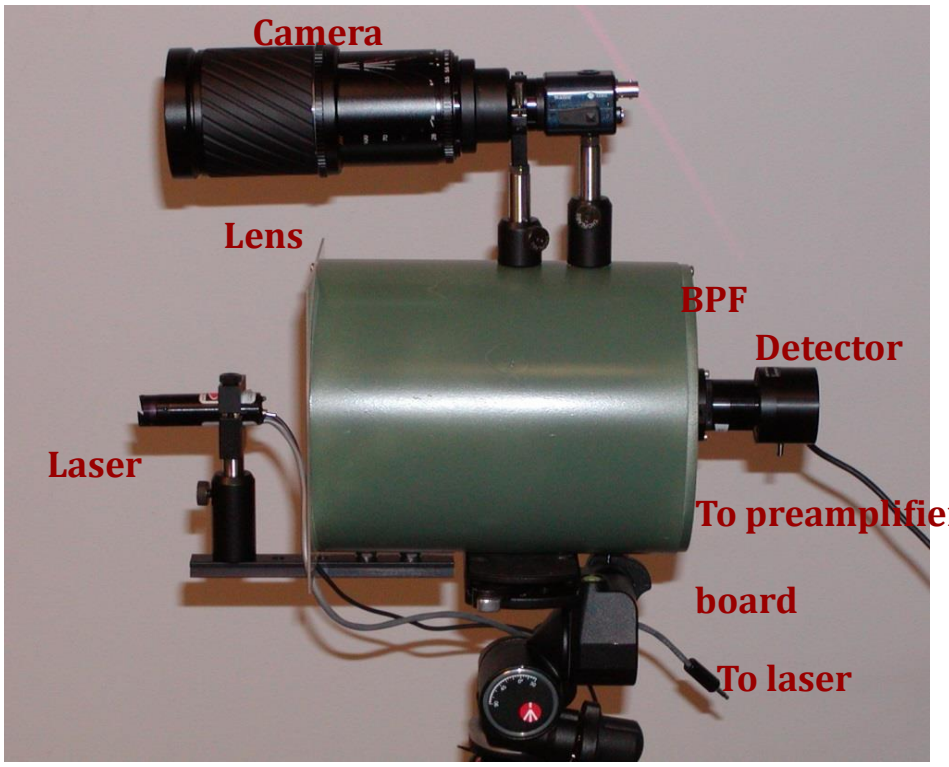

Figure 5-11: Front section of the receiver unit.

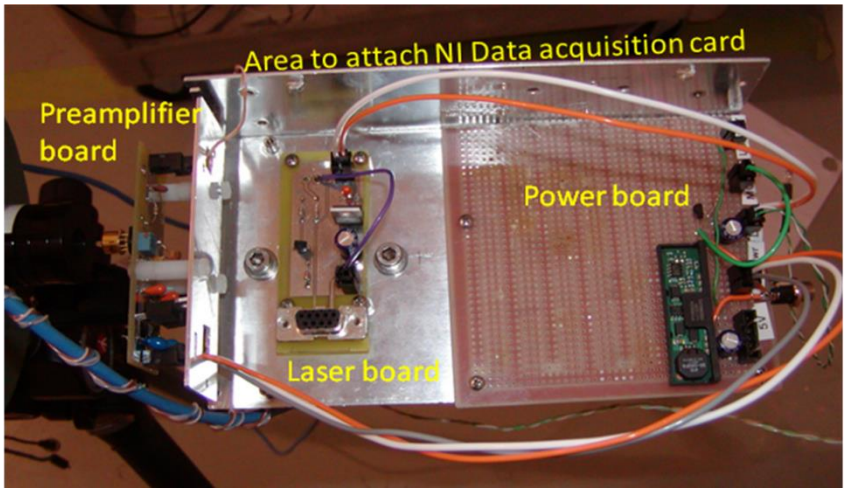

Figure 5-12: Rear end of the receiver unit, illustrating the improvements made towards making the high speed receiver system compact and portable.

The new receiver unit shown in Figure 5-11 and Figure 5-12 is highly compact and portable, compared to the one in Figure 5-3. Using the new transmitter and receiver, we were able to demonstrate optical communications up to 300 m. In Chapter 2 discussions on TIR and

evanescent waves, we illustrate that Equation 5.1 determines the penetration depth of evanescent waves for different wavelengths.

$$d = \frac{\lambda_i}{4\pi n_1 \sqrt{\sin^2 \Theta_i - \sin^2 \Theta_c}} \tag{5.1}$$

As seen in Figure 5-11the detector we ended up using is the, Newport's visible photodiode (918D) and an optical power meter (2935C) [57], however for S/N calculations we had used a different detector, Edmund optics 57-507 [12]. We were not able to obtain the complete details of the detector in Newport power meter, hence we were not able to perform S/N calculations as done in Chapter 2 Section 5 for other detectors. Also as we ran out of resources in the project, we were not able to perform the S/N ratio for the Newport power meter and will be a good thing to perform in future work.

The evanescent energy penetration depth is higher for longer interrogating wavelengths. Though we were never able to perform long range communication with higher wavelength, however on a simple short range (20 m) test we found that the modulation depth increased by five times using a 980 nm laser compared to 635 nm. Thus, we predict that using a 980-nm or a 1550-nm laser source in a receiver would significantly increase the communication range. The next chapter provides our conclusions with suggested future work to improve the existing technology.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

After reviewing the work done by other researchers and from our experience in developing MEMS-based CCRs, we realized that the orthogonality of the mirrors needs to be in the range of 1-30 arc second for long-range (1-2 km) line-of-sight optical communication. Assembling miniature mirrors with arc second degree of precision was very difficult, so we designed an amalgam of commercial TIR CCRs with a traditional MEMS chip. By using this approach, we preserved the advantage of the precise orthogonality of mirrors in the commercial CCR and bonded them to our MEMS chip. The modulating structures on the MEMS chip interacted with surface waves (evanescent waves) at the reflection point of the TIR CCR and attenuated the retroreflected signal. For our experiment, we selected a 12.7 mm, uncoated BK7 material CCR with a misalignment of 10 arc-seconds. We designed a 10 x 8 mm chip on an SOI wafer with an array of MEMS structures in the active area of 6.5 x 6.5 mm to interact with one side of the CCR. Eight variations of the MEMS chip were designed with different structure sizes (100 x 100 µm, 200 x 200 µm, and 500 x 500 µm), spring lengths, and numbers of springs that met our electrical requirements. The assembled chip had three electrodes, and we achieved movement of the MEMS plates either toward or away from the lid by applying 0-6 V (depending on the plate style). A 100 x 100 µm plate with a 33 x 34 array of MEMS plates on the chip required 178 µW of power to move toward the glass lid at 10 kHz. Once we were able to bond the glass lid and the SOI wafer containing the MEMS structure/plate, we were able to precisely

bond the SOI plus glass MEMS chip with high precision (10-30 arc-seconds) to any uncoated TIR-based CCR. Using a developed Michelson interferometer-feedback assembly method, we could see the retroreflected signal of the bonded CCR at a range of 1 km, which confirmed that the precision assembly methods were viable for creating long-range passive optical communication systems.

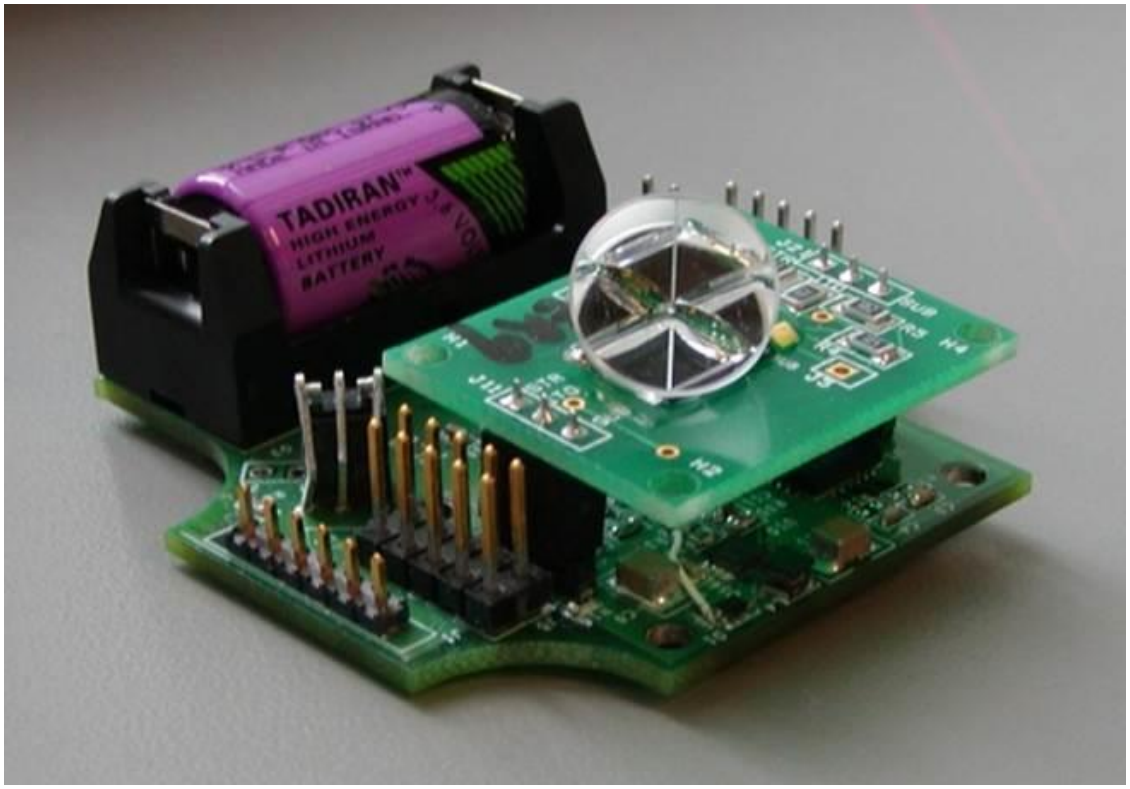

Figure 6-1: Assembled transmitter unit with temperature, humidity, and 2-axis magnetic sensors; microcontroller; infrared remote control receiver; field configuration jumpers; and a battery. The unit was housed in an IP-67 enclosure with transparent acrylic walls.

Next, we developed a sensor board containing temperature, humidity, and magnetic sensors; a microprocessor; and other required electronics to provide the modulation scheme and voltage to the MEMS chip. Using 635 nm as an interrogating laser source, we were able to demonstrate communication over 300 m with our transmitter, which contained the CCR and sensor board unit shown in Figure 6-1. Since the MEMS chip consumes very low power, this

transmitter unit can be used in other unattended sensor applications for an extended period of time.

From our calculations and experiments, we have shown that using a higher wavelength of 980 nm, 1550 nm or higher would give deeper penetration, interact more with the evanescent waves, and provide a higher modulation depth, all of which facilitate longer communication ranges. We also deduce that using a larger receiver aperture will increase the chances of capturing more retroreflected signals from distant transmitter units.

6.2 Future Work

During the project, we learnt a lot about optical communication system and discovered several potential improvements that would increase the communication range and reduce the size of the system. First, as we suggested earlier, our calculations indicated that we should use an eye-safe higher wavelength of 980 nm or 1550 nm for communication. A higher wavelength will provide higher contrast in retroreflected signals, provide greater penetration depth, and may allow us to position the MEMS structure a bit further from the glass lid. Along with this, if we performed detail optical simulations understanding what features would cause maximum scattering, then we can input that information and design MEMS structures

Second, in our experiments we used a 10 arc-second misaligned commercial CCR; however, 1 arc-second commercial CCRs are available in the market. The precise bonding of the CCR-MEMS chip, based on the Michelson-interferometry feedback method, cannot align better than the misalignment of the CCR itself, which means we could never bond the CCR-MEMS chip at better than 10 arc-seconds. Using a more precise CCR at the beginning gives us a better chance to align the CCR-MEMS chip more accurately.

Third, we suspected some bowing of the glass lid away from the MEMS structures, which might interfere with effective evanescent scattering at the glass interface. The glass bowing was noted as a potential problem, as several interference fringes were detected during interferometer bonding of the CCR/SOI chip, and perfectly flat samples should allow fringe nulling. One way to solve this problem would be to design SOI/glass lids with periodic bonding points within the array of MEMS plates to maintain a constant air gap between the glass and MEMS plates. This may prevent bowing, but it will decrease the fill factor of the MEMS structures.

Finally, since we were using a contact aligner, we were limited to 3 μm as our minimum feature size. If we use a stepper aligner, we can use a 1 μm (or smaller) minimum feature size, which would allow us to reduce the width of the springs, size of the release hole, pitch of release holes, busbar and plate size this will enable us design structures with low pull-in voltages and maintain high fill factor. Along with that using smaller structures would enable higher scattering efficiency too. Due to limited resources, we were not able to perform detailed signal to noise ratio measurements, this should be one of the measurements to perform in future.

Although the receiver unit seems portable, a more ruggedized, lightweight, and compact receiver unit can be developed; the sensor output, in the format of optical modulation, can be fed into a laptop (which can replace the instrumentations); and using LabVIEW-based software would allow the sensor data to be displayed more meaningfully.

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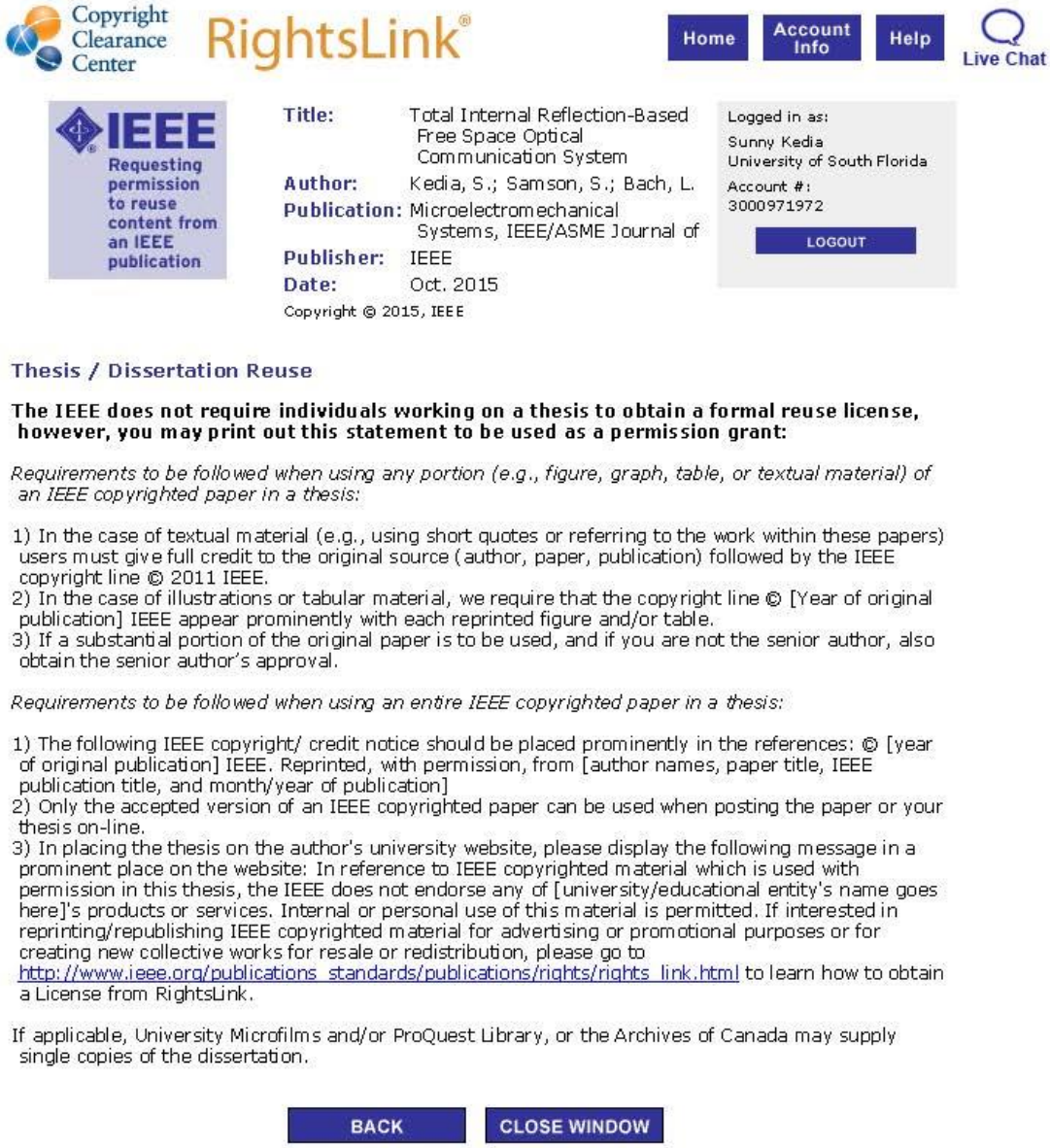

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ABOUT THE AUTHOR

Sunny Kedia received his Bachelor of Engineering (B.E) from Gandhi Institute of Technology and Management (GITAM), Visakhapatnam, India. He finished his Master's of Science (M.S) in electrical engineering from the University of South Florida (USF) in 2004, with a focus in printed circuit board (PCB) design/layout and sensor system development. He then joined USF's Center for Ocean Technology as a MEMS research engineer. At USF he developed expertise in MEMS sensor design and fabrication, with an emphasis on optical sensors, including corner cube retroreflector-based communication systems, optical spectrometer, beam scanner, and an accelerometer based on the principle of evanescent wave coupling. In 2007 he joined SRI International's St. Petersburg, FL, facility, where he developed sensors such as DC- DC converters and resettable circuit breakers. He joined the doctoral program at USF in 2008 and, along with his work at SRI, continued pursuing research in corner cube retroreflectors. In 2012 he moved to SRI headquarters in Menlo Park, CA, where he led efforts in microinverter and thermal sensor development. At SRI he has continued to strengthen his expertise in developing sensor circuitry for commercial optical, capacitive, and magnetic sensors and in developing sensors from scratch as necessary. He holds several patents, has published journal and conference papers, and has provided input as a reviewer on several journals and conference papers.